RVPW015 Current Mode PWM Controller

4-80VIN/132V/0.6Ω POWER MOSFET

FEATURES

- Suitable for PSR and SSR flyback/Boost/Buck
- PSR Feedback Minimum Sampling Time as Low as 0.4us
- CCM and DCM Modes are Compatible
- Integrated 132V/0.6Ω LDMOS
- Integrated Lossless Current Sampling
- Programmable Peak Current
- Programmable Power MOSFET Driving Speed
- Programmable Input Undervoltage and Overvoltage Protection
- Short Circuit Protection, and Over Temperature Protection
- Linearly Decrease of the Operating Frequency to Optimize Efficiency under Light-load Conditions
- Internal Feedforward Compensation Function
- Internal Soft Start and Slope Compensation
- Internal PSR Loop Control in CCM/DCM Mode
- Direct Optocoupler Interface
- Internal Loop Compensation and Output Diode Voltage Drop Temperature Compensation
- ESOP8 Strong Heat Dissipation Packaging

APPLICATIONS

- DCM/CCM Flyback Converter
- Industrial Power Conversion
- BMS Auxiliary Power Supplies
- POE Power Supplies
- Isolation Communication Power Supplies

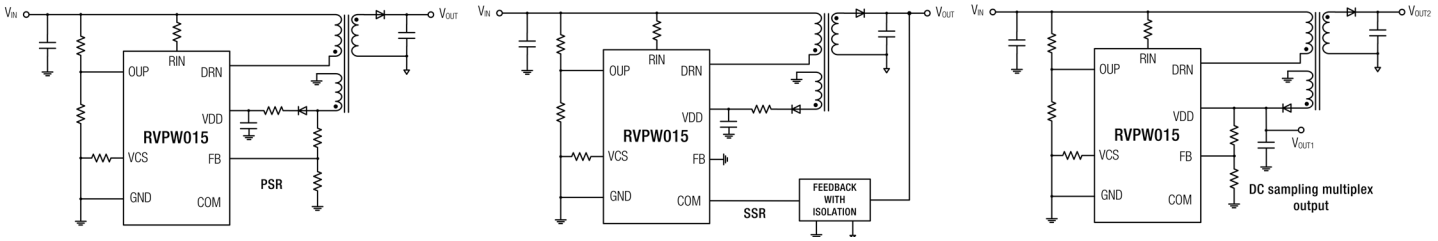
DESCRIPTION

RVPW015 is a highly integrated power control IC designed to support multiple power supply topologies, including Flyback, Boost, and Buck converters. It is compatible with various output voltage feedback methods such as Secondary-Side Regulation (SSR), Primary-Side Regulation (PSR), and resistive voltage divider feedback. PSR operation is supported at switching frequencies up to several hundred kHz. The internal output voltage sampling circuit is capable of operating in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), with a sampling time window requirement as short as 400ns. An integrated loop compensation circuit with fast dynamic response ensures excellent loop stability and rapid transient performance for the switching power supply. RVPW015 incorporates multiple control and protection functions, while requiring only minimal external components. It offers flexible design capabilities through configurable external resistors. A single resistor can be used to implement startup, feedforward compensation, and programmable turn-off speed control of the internal power MOSFET. Another resistor allows for programming the peak current of the power MOSFET, enabling a “lossless” current sensing method. With just two resistors, both input undervoltage protection (UVP) and input overvoltage protection (OVP) thresholds can be independently defined. The RVPW015 also integrates comprehensive protection features, including overload protection (OLP), output short-circuit protection (SCP), output overvoltage protection (OVP), and over-temperature protection (OTP). Once a fault condition is cleared, the chip automatically recovers, enhancing system robustness and maximizing the reliability of the power supply.

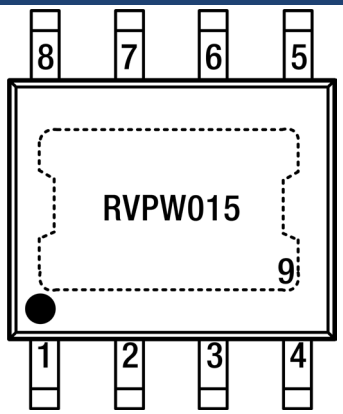
Device information

Part Number	Package	Weight(mg)	Dimension	QTY
RVPW015	ESOP8	77.00	5.0mm x 6.0mm	4000

SIMPLIFIED SCHEMATIC



PIN CONFIGURATION AND FUNCTIONS



Name	ESOP8 PIN No.	Type	Description
COM	1	I	In SSR operating mode, the optocoupler feedback pin controls both peak current and switching frequency through the voltage applied to it. This pin includes an internally integrated RC compensation circuit, allowing direct connection to an optocoupler without the need for additional external components.
VDD	2	P	Chip's power supply input, VDD, provides power to the internal control circuitry through an integrated low-dropout regulator (LDO), which generates an internal supply voltage, V_{CC}. The LDO operates in the linear region with a typical V_{CC} output of 5.3V, enters the dropout region when VDD falls close to V_{CC}, maintaining a typical dropout voltage of approximately 0.3V. VDD also features an internal voltage clamp with a clamping threshold of approximately 10V. If the current drawn by the clamp exceeds 5.3mA, the chip disables the internal power MOSFET and enters a self-recovery protection mode to ensure safe operation.
VCS	3	I	Peak Current Threshold Setting Pin. Connect a resistor (typically in the tens of kΩ range) from this pin to GND to set the maximum and minimum peak current thresholds in PSR mode. This configuration enables internal lossless current sensing.
GND	4	P	Ground Reference (GND). This pin serves as the signal ground for the internal control logic and also functions as the source terminal of the internal LDMOS device.
DRN	5	O	The drain of the internal LDMOS.
RIN	6	I	Connecting an external resistor to the V_{IN} enables startup control, adjustment of the power MOSFET shutdown speed, and implementation of feedforward compensation.
OUP	7	I	Input Overvoltage/Undervoltage Protection (Multiplexed Pin). This pin is used for both input undervoltage and overvoltage protection. Undervoltage protection threshold and recovery point can be configured by adjusting the resistor ratio of an external voltage divider. Overvoltage protection threshold is determined by the absolute values of the voltage divider resistors.
FB	8	I	Output Voltage Feedback Pin. This pin is used to sample the output voltage of the switching power supply. Sampling can be achieved either through the auxiliary winding of the transformer or directly using a resistor voltage divider. Sampling via the auxiliary winding enables isolated feedback, while the resistive divider method is suitable for non-isolated Flyback, Buck, or Boost converter applications. In Primary-Side Regulation (PSR) mode, the sampled voltage is processed by an internal error amplifier, which modulates the duty cycle of the power MOSFET to maintain a stable output voltage. In Secondary-Side Regulation (SSR) mode, the FB pin should be connected directly to GND.
EP	9	P	Exposed Pad (EP). Internally connected to GND. For optimal thermal performance, the EP should be soldered to a large ground plane. Note that the exposed pad is intended for heat dissipation only and is not used as an electrical signal connection point.

SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage Range of RIN to GND	V_{RIN}	-0.3	35	V
VDD to GND	V_{DD}	-0.3	13	V
DRN to GND	V_{DRN}	-1.3	132	V
FB to GND	V_{FB}	-0.5	6	V
Peak Current of FB to GND	$I_{FB(PEAK)}$		-2.5	mA
Other Pins to GND	V_{COM}, V_{OUP}, V_{CS}	-0.3	6	V
Maximum Operating Junction Temperature	T_{JMAX}		150	°C

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model HBM, per ESDA/JEDEC JS-001-2023; (Zap 1 pulse, Interval :>=0.1S)	±1500	V
		Charged device model CDM, per ESDA/JEDEC JS-002-2022	±1000	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Resistance

Packaging	θ_{JA}	Ψ_{JT}	UNIT
ESOP8	51.9	6.5	°C/W

Note: The measurements were made on a test plate with a thickness of 1oz and an area of 7.62 x 11.43CM

Thermal Information

		MIN	NOM	MAX	UNIT
Junction-to-ambient thermal resistance	$R\theta_{JA}$		51.9		°C/W
Junction-to-top characterization parameter	Ψ_{JT}		6.5		°C/W

Note: Measured on a copper thickness of 1oz 7.62cm x 11.43cm test plate.

Recommended Operatings Conditions

		MIN	NOM	MAX	UNIT
Power MOSFET Drain Voltage	V_{DRN}			125	V
VDD Input Voltage	V_{DD}	4		10	V
VCS External Resistor	R_{CS}	12			kΩ
RIN External Resistor	R_{IN}			1	MΩ
FB Current	I_{FB}	-2			mA
Operating Ambient Temperature	T_A	-40		125	°C

Electrical Characteristics

Unless otherwise specified, the following parameters were measured under the condition of V_{DD}=7V and temperature T=25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
$V_{DD(ON)}$	VDD turn on threshold	V_{DD} rising	3.1	3.3	3.5	V
$V_{DD(OFF)}$	VDD turn off threshold	V_{DD} falling	2.8	3.0	3.2	V
$I_{VDD(ON)}$	VDD turn on current	V_{DD} rising		61	100	uA
$I_{VDD(OP)}$	Operating current at full load in SSR mode	Connect COM to 6.8kΩ to GND, V_{FB}=0V	1.1	1.9	2.7	mA
$I_{VDD(UVP)}$	Operating current under input voltage	OUP=0V		143	200	uA
$V_{DD(DMAX)}$	MOSFET for starting up supply voltage@D_{MAX}	F_{DRN}=330kHz, 80% duty cycle	3.1	3.8	5.0	V
$V_{BV(DIODE)}$	Break voltage of anti reflow diode		37			V
$V_{DD(OVP)}$	VDD overvoltage shutdown threshold	V_{DD} rising	9.5	10	10.8	V
$I_{VDD(OVP)}$	VDD absorbs current during overvoltage protection	V_{DD}= $V_{DD(OVP)}$	4.5	5.3	6.5	mA
RIN						
V_{ZB}	MOSFET for starting up bias voltage	I_{RIN}=1uA	6.0	6.9	8.0	V
$R_{IN(IN)}$	Input resistance			100		kΩ
VCS						
$V_{CS(MAX)}$	Maximum threshold voltage		1.85	2.00	2.15	V
$V_{CS(MIN)}$	Minimum threshold voltage	PSR mode	225	250	275	mV
		SSR mode	80	100	120	mV
k_{CS}	Proportional coefficient between peak current of power MOSFET and VCS current		9300	11000	12700	A/A
$D_{35\%}$	Initial duty cycle of adding slope compensation			35		%
OUP						
$V_{OUP(ON)}$	Undervoltage protection turn on voltage		1.9	2.0	2.1	V
$V_{OUP(OFF)}$	Undervoltage protection turn off voltage		1.67	1.75	1.83	V
$V_{OUP(OC)}$	Input overcurrent protection clamp voltage	I_{OUP}=50uA injected into OUP pin	2.1	2.2	2.4	V
$I_{OUP(OFF)}$	Input overcurrent protection comparison current	I_{OUP} gradually increasing	92	100	108	uA
$I_{OUP(ON)}$	Input overcurrent protection recovery comparison current	I_{OUP} gradually decreasing	83	90	97	uA
FB						
$V_{REF(REG)}$	Reference voltage of EA		1.97	2.00	2.03	V
A_V	Low frequency gain of EA			1400		V/V
$T_{D(SAMP)}$	Delay time of sampling			252	350	nS
K_{VTC}	The temperature coefficient of temperature compensation voltage			3.5		mV/°C
I_{FB}	Pin input current	When the FB pin is used as a feedback voltage		-40		nA
		When COM is used as feedback, the FB pull-up current		20		uA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
COM						
$V_{COM(OPEN)}$	Open loop voltage		5.0	5.3	5.6	V
$V_{COM(OLP)}$	Threshold voltage of OLP	VDD≥5.3V	4.0	4.5	5.0	V
		VDD<5.3V		VDD - 0.8		V
I_{COM}	Maximum output current of COM	V_{COM}=0V	1.06	1.3	1.59	mA
$V_{COM(IMAX)}$	Pin voltage at maximum peak current	COM rises until V_{CS}=$V_{CS(MAX)}$	2.60	2.75	2.90	V
t_{SS}	Soft start time	V_{COM} rising	2.6	3.6	4.6	mS
DRN						
$R_{DS(ON)}$	MOSFET on-state resistance	I_{DS}=0.8A, T=25°C		600		mΩ
		I_{DS}=0.8A, T=125°C		900		mΩ
f_{OSC}	Maximum operating frequency	Frequency without simulated downsampling	300	330	360	kHz
f_{MIN}	Minimum operating frequency		6	9	12	kHz
D_{MAX}	Maximum duty cycle		75	80	85	%
$t_{ON(MIN)}$	Minimum conduction time	VCS suspended, drain connected to a 120Ω pull-up resistor, pull-up voltage is 24V		250		nS
$t_{ON(MAX)}$	Maximum conduction time		2.15	2.4	2.65	uS
OTHER PROTECTIVE FUNCTIONS						
T_{SHDN}	Over temperature protection threshold		148	163	178	°C
$T_{SHDN(HYS)}$	Over temperature protection hysteresis			18		°C
$t_{DLY(OLP)}$	OLP trigger time	From V_{COM}>$V_{COM(OLP)}$ to entering protection		55		mS
t_{rest}	Rest time after self recovery protection			1.4		S

Typical Characteristics

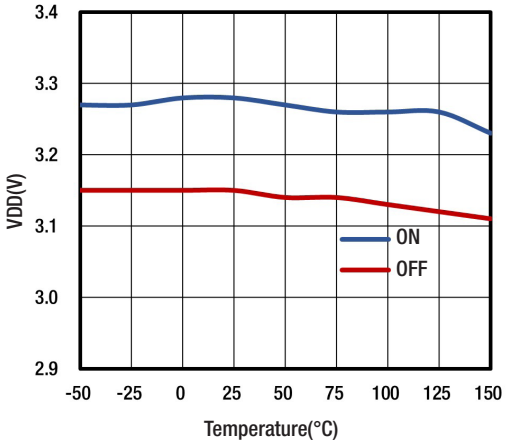


Fig. 1 $V_{DD(ON)}$ and $V_{DD(OFF)}$ vs Temperature

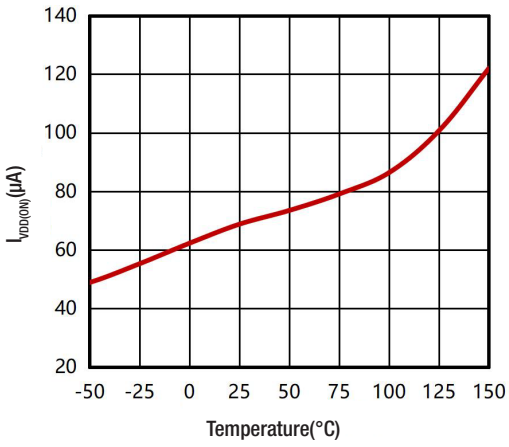


Fig. 2 $I_{VDD(ON)}$ vs Temperature

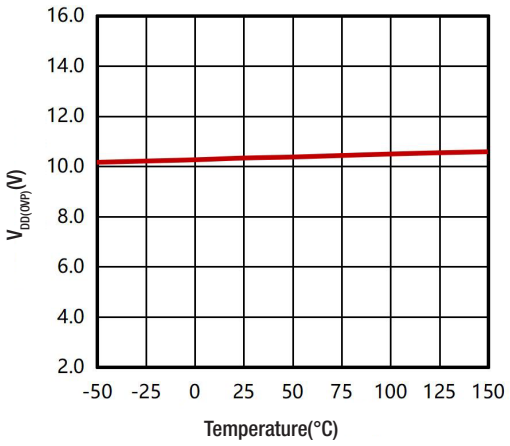


Fig. 3 $V_{DD(OVP)}$ vs Temperature

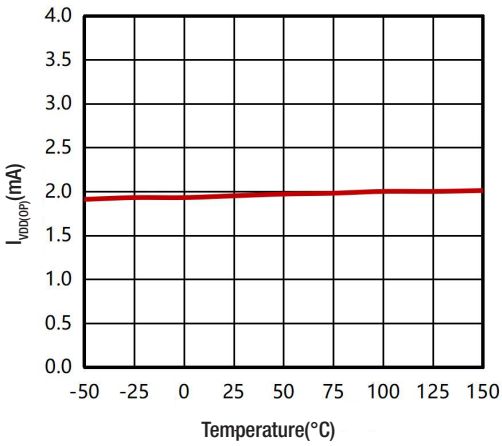


Fig. 4 $I_{VDD(OP)}$ vs Temperature

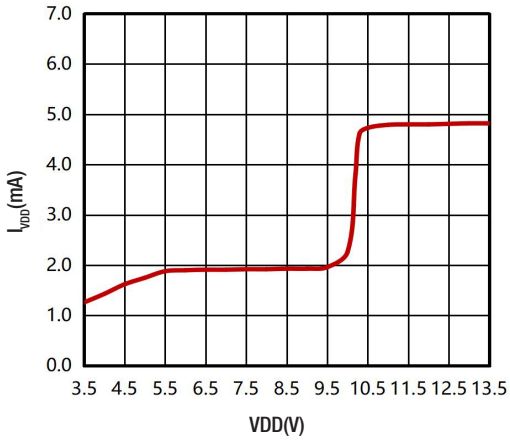


Fig. 5 I_{VDD} vs V_{DD}

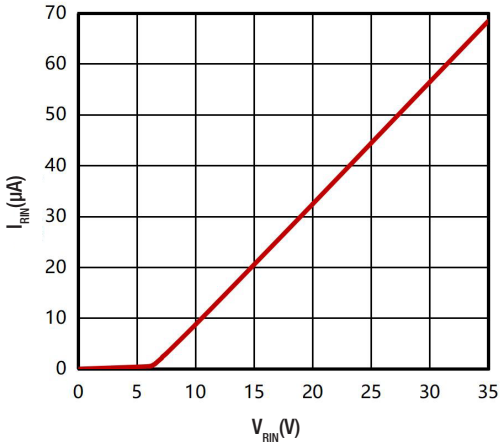


Fig. 6 I_{RIN} vs V_{RIN}

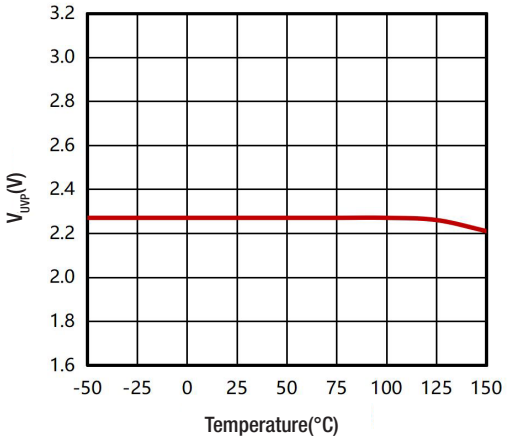


Fig. 7 $V_{OUP(OC)}$ vs Temperature

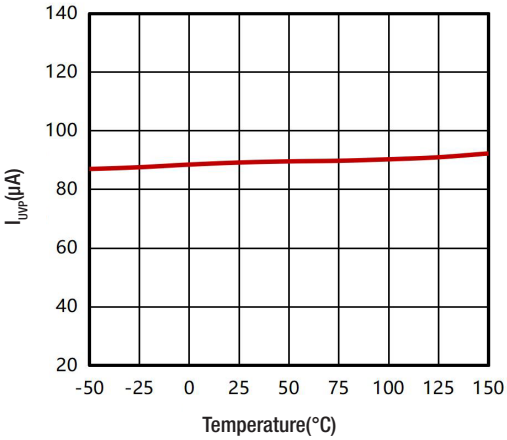


Fig. 8 $I_{OUP(ON)}$ vs Temperature

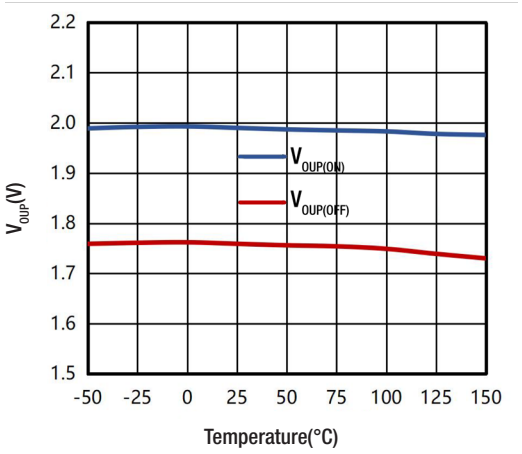


Fig. 9 $V_{OUP(ON)}$ and $V_{OUP(OFF)}$ vs Temperature

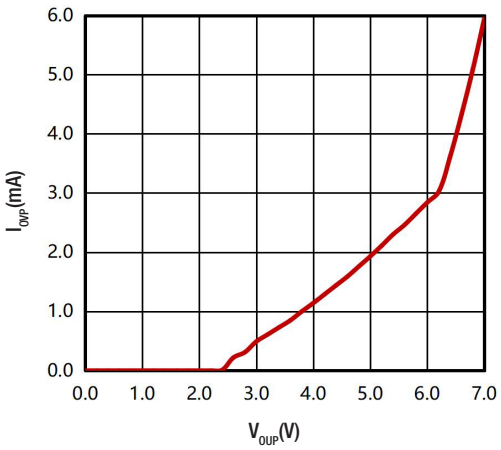


Fig. 10 I_{OUP} vs V_{OUP}

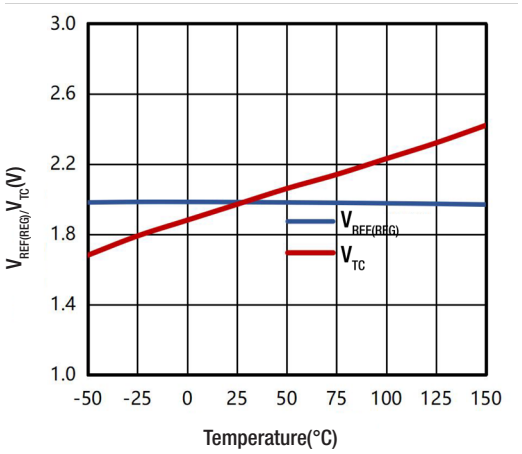


Fig. 11 $V_{REF(REG)}$/V_{TC} vs Temperature

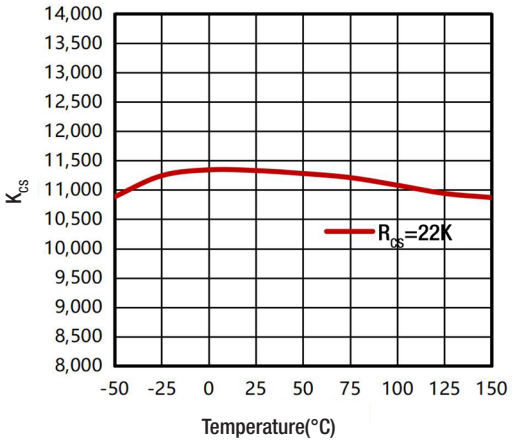


Fig. 12 K_{CS} vs Temperature

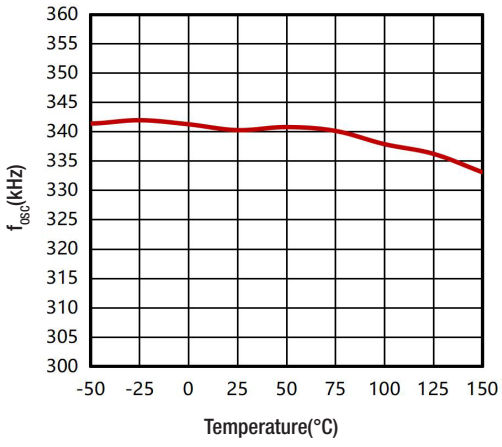


Fig. 13 f_{OSC} vs Temperature

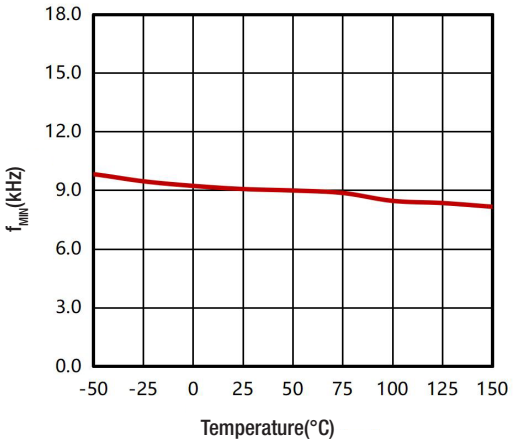


Fig. 14 f_{MIN} vs Temperature

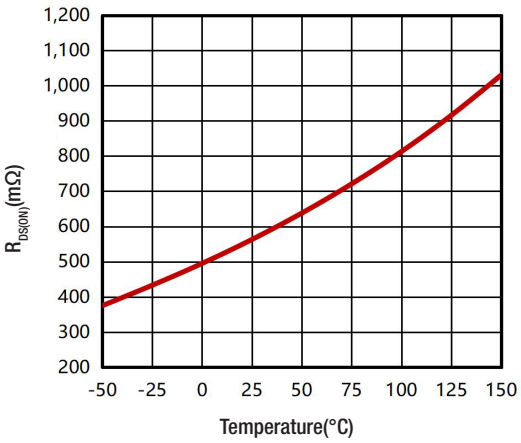


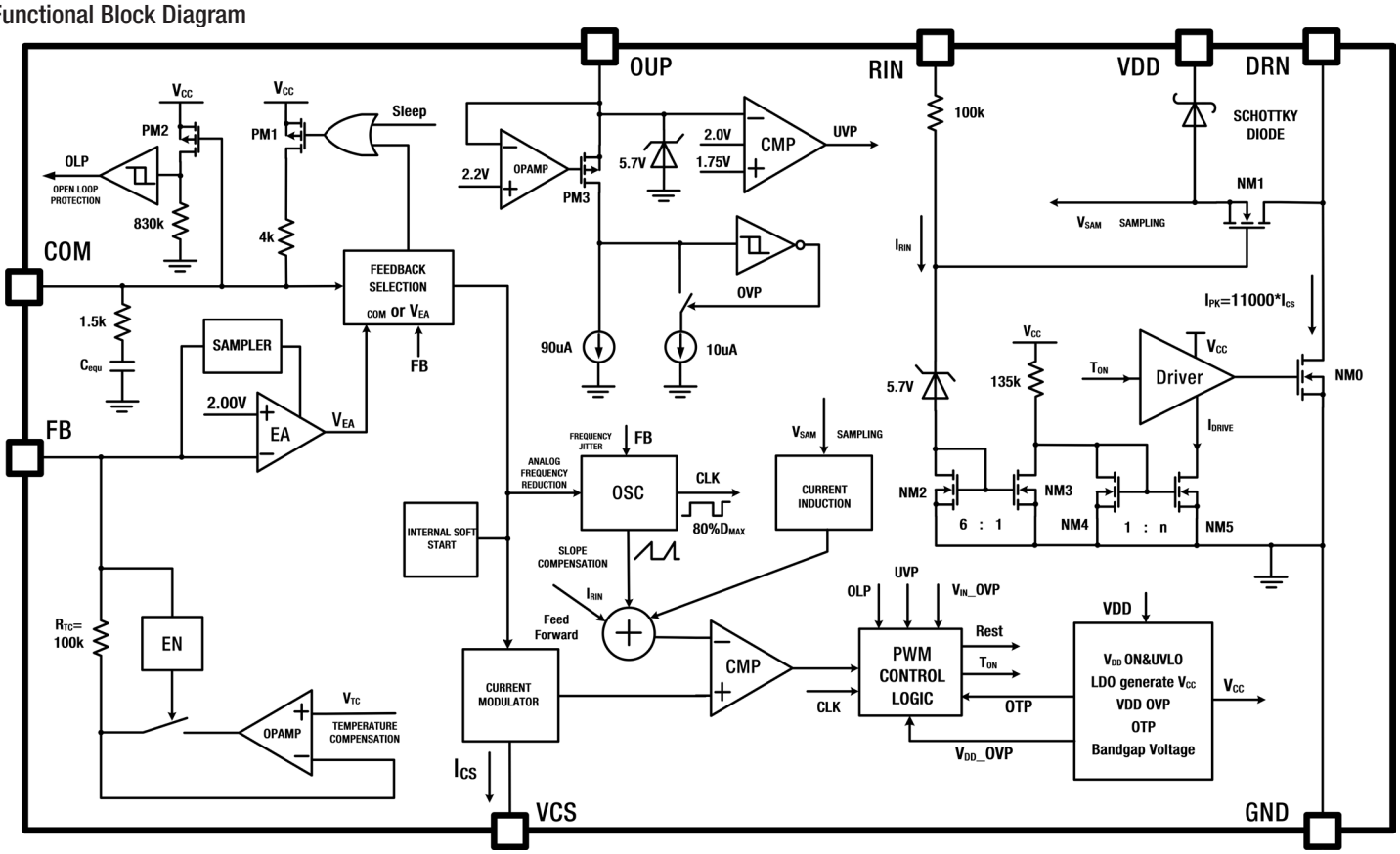
Fig. 15 $R_{DS(ON)}$ vs Temperature

FUNCTIONS AND PRINCIPLES

Overview

RVPW015 is a current-mode PWM converter that integrates both control circuitry and a power MOSFET on a single chip using advanced BCD technology. It supports multiple power supply topologies-including Flyback, Buck, and Boost-with output power up to 10W. RVPW015 features two feedback pins, COM and FB, offering flexibility for both isolated and non-isolated designs. For isolated Flyback power supplies requiring high output voltage accuracy, secondary-side regulation (SSR) can be implemented using components such as a TL431 and optocoupler. In this configuration, the COM pin is used to regulate the output voltage via closed-loop feedback. For cost-sensitive applications that do not require high output voltage precision, an optocoupler-free primary-side regulation (PSR) method can be used. In PSR mode, the FB pin samples the voltage from the auxiliary winding of the transformer to regulate the output voltage. In non-isolated applications-such as Buck or Boost converters-the output voltage can be directly sampled through a resistor divider and fed to the FB pin for regulation. RVPW015 supports operation in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), enabling compact power supply designs. Its flexibility and wide input voltage range make it ideal for use in a variety of applications, including IGBT-based motor drives, industrial automation systems, and medical instruments.

Functional Block Diagram



Feature Description

Function and Resistance Design of External Resistor R_{IN}

As shown in Figure 16, a resistor R_{IN} is connected between the RIN pin of the RVPW015 and the converter's input voltage V_{IN}. This resistor performs three key functions. First, it provides the bias current required to activate the internal startup MOSFET (NM1). Second, it programs the turn-off speed of the internal power MOSFET (NM0). Third, it enables a feedforward compensation mechanism.

Startup and power supply: R_{IN} delivers bias current to a 5.7V Zener diode and to NM2, which is connected gate-to-source. The sum of the Zener breakdown voltage and the gate-to-source voltage of NM2 is approximately 6.9V. This voltage provides the necessary bias for enabling the startup MOSFET NM1. Once NM1 is turned on, it allows startup current to flow from the drain pin (DRN) of the main power MOSFET NM0, through NM1 and a Schottky diode, to charge the VDD capacitor. After the converter's output voltage has been properly established, it is recommended to power the VDD pin through the auxiliary winding of the transformer. This transition is necessary to reduce power loss, as the internal startup circuit consumes considerable energy during operation. To ensure the startup circuit is fully disabled, the VDD voltage must exceed 6V. VDD pin is also equipped with internal voltage clamp and overvoltage protection features. The clamping voltage is set at 10V, and if the current absorbed by the clamp exceeds 5mA, overvoltage protection is triggered, causing the chip to enter a protection state. In flyback converter applications, this protection mechanism can be utilized as an output overvoltage protection feature by taking advantage of the proportional relationship between the auxiliary winding voltage and the secondary output voltage. Regarding the switching behavior of the internal power MOSFET NM0, the current flowing into the RIN pin, denoted as I_{RIN}, is used to generate the gate driving current I_{DRIVE}. The relationship between I_{RIN} and I_{DRIVE} determines the switching speed of NM0, which can be adjusted accordingly through the value of R_{IN} and their relationship is:

$$\frac{I_{DRIVE}}{n} = \frac{V_{CC} - V_{GS4}}{135k\Omega} - \frac{1}{6} \times \frac{V_{IN} - 5.7 - V_{GS2}}{R_{IN} + 100k\Omega}$$

In the equation described above, V_{CC}=5.3V and $V_{GS2} \approx V_{GS4} \approx 1.2V$. When R_{IN}=330kΩ, and the equation yields zero, I_{DRIVE}=0 occurs at an input voltage of V_{IN}= 85V. At this point, the gate driver circuit turns the internal power MOSFET (NM0) on and off using only its inherent driving capability, resulting in the slowest turn-off speed. When I_{DRIVE}>0, the shutdown speed of NM0 increases accordingly. From the equation, two key relationships can be observed: By adjusting the R_{IN} value, the shutdown speed of NM0 can be programmed. A larger R_{IN} results in a faster turn-off speed. As the input voltage increases, I_{DRIVE} decreases, causing a slower NM0 turn-off. This behavior helps suppress voltage spikes caused by leakage inductance under high input voltage conditions.

Feedforward Compensation Function and RIN Resistor Design: RVPW015 incorporates a feedforward compensation mechanism by proportionally mirroring the current I_{RIN} from NM2 to generate a feedforward compensation current. This current is superimposed with both the sampling current of the power MOSFET NM0 and the slope compensation current, and the combined signal is used as the input to the PWM comparator. As the input voltage increases, the feedforward compensation current also increases. This behavior helps to reduce variation in the overcurrent threshold between high and low input voltages, which would otherwise result from delays in the PWM comparator and gate driver. Regarding the design of the R_{IN} resistor, a 100 kΩ resistor is already connected in series internally within the chip. This built-in resistor serves two purposes. First, it absorbs part of the input voltage, ensuring that even if an ultra-small external R_{IN} resistor is selected, there is no risk of inadequate voltage isolation or insulation. Second, in low input voltage applications, this internal resistor allows designers to consider omitting the external R_{IN} altogether, simplifying the circuit. There is no strict requirement on the value of R_{IN} for the startup biasing of NM1, as the startup circuit is designed to be tolerant. Therefore, the choice of R_{IN} is mainly determined by the desired trade-off between the turn-off speed of the power MOSFET NM0 and the strength of the feedforward compensation effect. In typical applications, the value of R_{IN} is selected within the range of several hundred kilo-ohms to 1 MΩ.

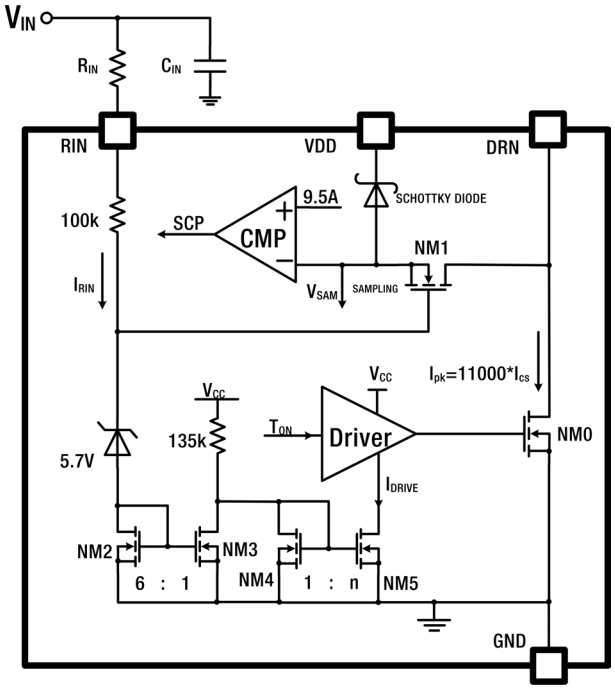


Fig. 16 Startup and turn-off speed

Input Over/Under Voltage Protection

As shown in figure 17, the input overvoltage and undervoltage protection functions of the RVPW015 are implemented through a single pin OUP. The threshold voltages for both protections can be programmed based on application requirements. The operating principle is as follows: When the voltage at the OUP pin is less than 2.2V, the pin draws no current. Under this condition, the turn-on and turn-off thresholds for input undervoltage protection V_{IN} can be easily calculated using the following formulas:

$$V_{INON(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2V$$

$$V_{INOFF(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 1.75V$$

When the voltage at the OUP pin exceeds 2.2V, the pin begins to draw current and maintains this voltage level until the current exceeds 100μA. At this point, the condition is recognized as an OUP input overcurrent, triggering the chip to stop switching the power MOSFET NM0 and enter a protection state. As the input voltage decreases and the current drawn by the OUP pin falls below 90μA, the chip automatically exits the protection mode and resumes normal operation. The input overvoltage protection threshold and recovery voltage can be calculated using the following formulas:

$$V_{INOFF(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2.2V + 100\mu A \times R_{OU2}$$

$$V_{INON(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2.2V + 90\mu A \times R_{OU2}$$

When designing the resistance values of R_{OU1} and R_{OU2}, a more practical formula can be obtained to quickly determine the resistance:

$$R_{OU2} = \frac{V_{INOFF(OVP)} - 1.1 \times V_{INON(UVP)}}{100\mu A}$$

As long as the operating range of the input voltage of the converter is determined, R_{OU2} can be calculated, and then combined with the undervoltage protection formula, R_{OU1} can be calculated.

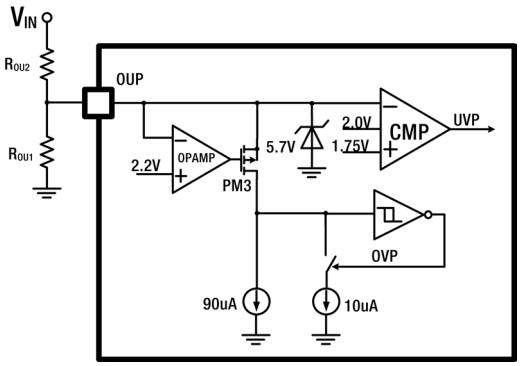


Fig. 17 Input Over/Under Voltage Protection

Mode Selection of Multiple Voltage Feedback Methods

RVPW015 supports multiple output voltage feedback modes, including secondary-side feedback (SSR) using optocoupler isolation, primary-side feedback (PSR) using transformer auxiliary windings, and direct resistive voltage divider sampling. In SSR mode, the closed-loop feedback signal is introduced through the COM pin. In PSR and resistive divider feedback modes, the closed-loop feedback is obtained via the FB pin by sensing the output voltage of the converter. Operating feedback mode is automatically determined based on the chip's peripheral connections and is selected during the first 12 switching cycles after power-up or after a protection event that causes a restart. If the COM pin is connected and used for feedback, the voltage on COM is treated as the duty cycle modulation voltage and is directly compared in the internal PWM control logic. Alternatively, if the FB pin is used for feedback, the output voltage V_{EA} of the internal error amplifier (EA) becomes the duty cycle modulation voltage for the PWM comparator. Therefore, selecting the correct feedback mode requires careful design of the external circuit and appropriate connection of the COM or FB pin, depending on whether SSR, PSR, or resistive feedback is being implemented.

Feedback method	COM pin	FB pin
Optocoupler feedback SSR	Connect to optocoupler	Connect to GND
Winding feedback PSR	Float	Auxiliary winding resistance voltage divider terminal
Direct sampling of resistive subdivision	Connect to GND	Resistance voltage divider terminal of the converter output

PWM and PFM Control

Current Sampling: RVPW015 implements current sampling by detecting the conduction voltage drop across the power MOSFET NM0. This voltage is measured at the source of the startup MOSFET NM1. It is then replicated by an internal operational amplifier to a sampling MOSFET that is of the same type as NM0 but has a higher internal resistance. As a result, a proportional induced current is generated on the sampling MOSFET, reflecting the peak current I_{PK} of NM0.

Current Modulator: Pulse-width modulation voltage-either V_{COM} or V_{EA}, depending on the feedback mode-produces a corresponding modulation current across an external resistor connected to the VCS pin. As shown in Figure 18, the relationship between V_{COM}, V_{EA}, and V_{CS} is continuous. As the modulation voltage varies, V_{CS} tracks its changes, generating a control current through the resistor, which in turn adjusts the peak current of NM0. This directly regulates the output voltage of the converter. When V_{COM} or V_{EA} exceeds 2.75V, V_{CS} reaches its maximum value, $V_{CS(MAX)}$, thus limiting the maximum peak current of NM0. The minimum voltage $V_{CS(MIN)}$ differs by feedback mode: in SSR mode, it is 100mV; in PSR mode, it is 250mV. A higher $V_{CS(MIN)}$ allows for a longer demagnetization period, which improves the accuracy of output voltage sampling at the FB pin. However, it also increases the minimum energy transferred per switching cycle, which may require additional dummy loading to prevent output voltage drift under no-load conditions.

PWM Control: Modulation current generated by V_{COM} or V_{EA} is applied as the positive input to the internal PWM comparator. The negative input consists of the sum of the sampled current proportional to I_{PK}, the slope compensation current, and the feedforward compensation current. The output of the comparator determines the gate drive signal of NM0, thus regulating the pulse width to maintain the output voltage at its rated value. RVPW015 supports a maximum duty cycle of 80%. To suppress subharmonic oscillation, which can occur when duty cycle exceeds 50%, the chip integrates internal slope compensation. This compensation is implemented by generating a ramp current synchronized with the oscillator's ramp voltage. To reduce the adverse impact of slope compensation on load capacity at low input voltages, ramp current is only activated when the duty cycle exceeds 35%; below this threshold, slope compensation is not applied. At the maximum duty cycle of 80%, the ramp compensation current also reaches its peak value.

PFM Control (Light Load Efficiency Mode): To enhance efficiency under light-load conditions and reduce no-load power consumption, RVPW015 includes a frequency reduction mode based on pulse frequency modulation (PFM). As the converter load decreases, the modulation voltage V_{COM} or V_{EA} decreases accordingly. When the load drops to approximately 30% of the rated maximum output power, the switching frequency begins to decrease in proportion to the declining modulation voltage. The minimum operating frequency in this mode is limited to F_{MIN}=9kHz. The frequency variation curve as a function of V_{COM} and V_{EA} is illustrated by the red solid line in Figure 18.

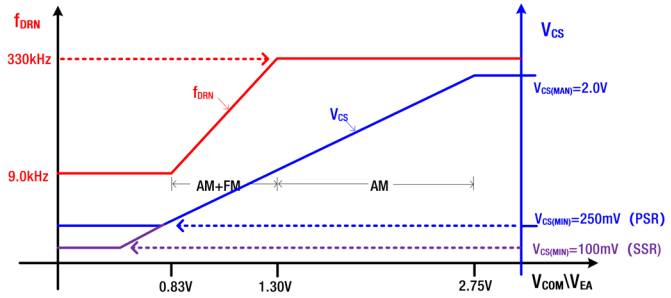


Fig. 18 Variation Curves of Switching Frequency and Peak Current Modulation with V_{COM} and V_{EA}

Peak Current Setting of Power MOSFET

The peak current of the power MOSFET (NM0) in the RVPW015 is regulated by a current modulator, which adjusts the current I_{CS} based on the voltage at the VCS[3] pin and the external resistor R_{CS}; The drain current of the power MOSFET is 11,000 times the value of I_{CS}.

The value of R_{CS} can be calculated using the following formula:

$$R_{CS} = 11000 \times \frac{V_{CS(MAX)}}{I_{PK}}$$

Among them: $V_{CS(MAX)}$ is the maximum threshold voltage of the VCS pin, with a typical value of 2V;
I_{PK} is the maximum peak current of the primary winding of the flyback converter.

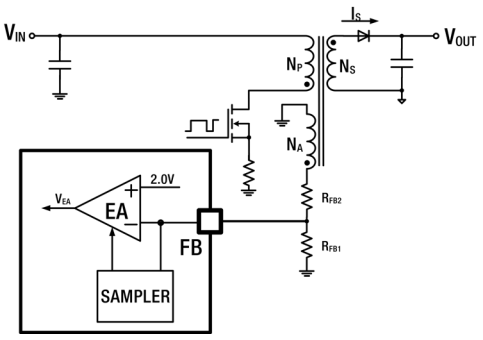


Fig. 19

FB Pin PSR Feedback Voltage Sampling

RVPW015 can sense the output voltage of the switching power supply by monitoring the auxiliary winding of the transformer. A sampling resistor connected to this auxiliary winding is tied to the FB pin. During the transformer's demagnetization phase, the voltage across the auxiliary winding is sampled and used as the negative input to the internal error amplifier (EA). This voltage is then differentially amplified against a fixed positive reference voltage, $V_{REF(REG)}$= 2V, to generate the duty cycle modulation voltage, V_{EA} which is used to regulate the duty cycle of the converter. As illustrated in Figure 19, this process ensures that the converter adjusts its switching behavior to maintain output voltage regulation. The waveform of the auxiliary winding voltage during this process is shown in Figure 20. Once the control loop reaches a steady state, the sampled voltage at the FB pin stabilizes at the 2V reference voltage of the EA. Based on this steady-state condition, the output voltage of the converter can be calculated from the relationship between the auxiliary winding, the feedback resistors, and the output parameters.

$$V_{FB} = (V_{OUT} + V_F + I_S R_S) \times \frac{N_A}{N_S} \times \frac{R_{FB1}}{R_{FB1} + R_{FB2}} = 2V$$

$$\text{Therefore } V_{OUT} = \times \frac{N_S}{N_A} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times 2V - (V_F + I_S R_S),$$

Let N_S and N_A represent the number of turns in the transformer's secondary output winding and primary auxiliary winding, respectively. The resistors R_{FB1} and R_{FB2} form the sampling network connected to the auxiliary winding. V_F is the forward voltage drop across the output diode, I_S is the secondary-side output current, and R_S is the total resistance in the secondary output circuit. According to the voltage calculation formula, the term $I_S R_S$ contributes to load regulation error in the switching power supply and should be minimized where possible. To address this, the RVPW015 samples the voltage at the FB pin at the end of the transformer's demagnetization stage-when I_S is at its lowest. In Discontinuous Conduction Mode (DCM), where I_S=0 at the end of demagnetization, the output voltage is not affected by the $I_S R_S$ term, enabling higher output voltage accuracy. Therefore, for applications requiring precise output regulation, DCM operation is preferred. In Continuous Conduction Mode (CCM), however, residual current I_S during demagnetization still contributes to voltage drop across R_S, causing the output voltage to decrease as load increases.

Regardless of whether the converter operates in DCM or CCM, a sudden drop of 20% in the FB voltage is used to detect the end of the demagnetization phase. Upon this detection, the system latches the output voltage of the error amplifier (EA). Because EA is designed with a built-in delay, its output does not respond immediately to the sudden voltage drop at FB. Thus, the latched value corresponds to the steady-state FB voltage just before the transient, ensuring accurate sampling. In the initial demagnetization phase after NM0 turns off, resonant ringing caused by leakage inductance and parasitic capacitance in the transformer may introduce noise on the FB signal. To prevent incorrect sampling due to these oscillations, the sampler includes a delay time $T_{D(SAMP)}$, during which it remains inactive. Sampling is only performed during the defined window T_{SAMP}, where it is required that the resonance-induced peak-to-peak FB voltage variation be limited to within 20% (approximately 400mV) of the FB voltage. When converting this requirement to the auxiliary winding side, the resistor divider ratio must be taken into account. It is strongly recommended not to place filter capacitors in parallel to GND on the FB pin, as this can distort the voltage waveform and compromise the sampling accuracy, especially in high-frequency PSR systems operating at several hundred kHz. Under light-load conditions, the demagnetization time is short, and even the parasitic capacitance of an oscilloscope probe may alter the FB waveform and affect the output voltage.

To ensure both waveform integrity and acceptable power consumption of the feedback network, the recommended range for R_{FB1} is between 2.5kΩ and 6kΩ, with a typical value of 4kΩ.

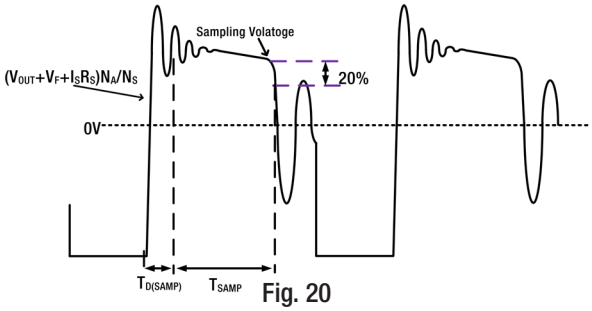


Fig. 20

Output Diode Temperature Compensation

RVPW015 includes a selectable temperature compensation feature, as illustrated in Figure 21. During the soft-start phase, the controller monitors the FB pin when the power MOSFET turns on. If no negative voltage is detected at the FB pin during this time, the temperature compensation enable switch remains open, disabling the temperature compensation function. Conversely, if a negative voltage is detected at FB during the MOSFET's turn-on phase, the enable switch closes, activating the temperature compensation circuit. When enabled, a positive temperature coefficient voltage V_{TC} is generated and buffered through a unity-gain amplifier. This voltage is then connected to the FB pin through a resistor R_{TC}=100kΩ. The voltage V_{TC} has a positive temperature coefficient of 3.5mV/°C, and at room temperature, V_{TC}= $V_{REF(REG)}$. This allows the RVPW015 to implement temperature compensation in primary-side regulation (PSR) flyback power supply applications. The degree of compensation is determined by the FB pin's voltage divider configuration, specifically the value of R_{FB2}. A calculation for determining R_{FB2} follows below.

$$V_{OUT} = \frac{N_S}{N_A} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times V_{REF(REG)} - \{\frac{N_S}{N_A} \times \frac{R_{FB2}}{R_{TC}} [V_{TC} - V_{REF(REG)}] + V_D\}$$

In the above equation, N_S and N_A represent the number of turns in the secondary and auxiliary windings of the transformer, respectively. V_D denotes the forward voltage drop across the output diode junction. To minimize the temperature coefficient of the output voltage, we set the derivative of the output voltage with respect to temperature to zero. This yields the condition for achieving temperature stability:

$$R_{FB2} = \frac{N_A}{N_S} \times \frac{\triangle V_D}{577.5mV} \times 100k\Omega$$

Let ΔV_D represent the change in the forward voltage drop of the output diode across the temperature range of -40°C to 125°C. To compensate for this temperature-induced variation in the output voltage, the appropriate value of R_{FB2} should be determined based on ΔV_D and this transformer turn the ratio N_S/N_A. Once R_{FB2} is established to achieve the desired temperature compensation, the value of R_{FB1} can then be calculated to set the target output voltage according to the required voltage division ratio.

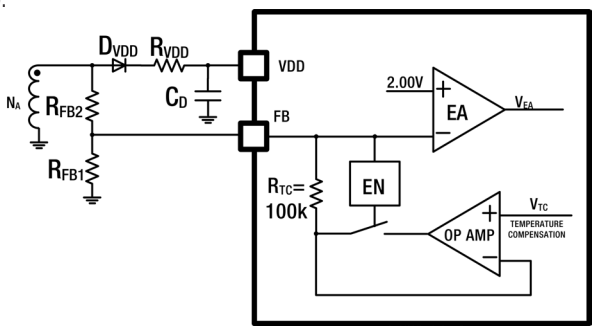


Fig. 21

OPERATION MODE

Feedback Port and Soft Start Up

As shown in Figure 22, when the chip is powered on or recovers from a protection condition, it enters a feedback mode selection stage during the first 12 switching cycles (from t_1 to t_2,) followed by a soft start phase (from t_2 to t_3). During the mode selection stage, the COM pin is pulled to approximately 2.4V, serving solely as a detection voltage for determining the type of feedback used. At this time, the internal PWM comparator threshold is intentionally limited to prevent high peak current in the power MOSFET. If an optocoupler is connected to the COM pin (indicating optocoupler feedback mode), the 2.4V detection voltage is maintained for the full 12-cycle duration. If the FB pin is used for primary-side regulation (PSR) feedback, and the controller detects this mode, the detection voltage lasts for only 2 switching cycles before exiting the mode selection stage. In optocoupler feedback mode, once the feedback mode has been determined, the internal soft-start voltage begins to rise gradually. This results in a controlled increase in duty cycle, ensuring a smooth startup without overshoot.

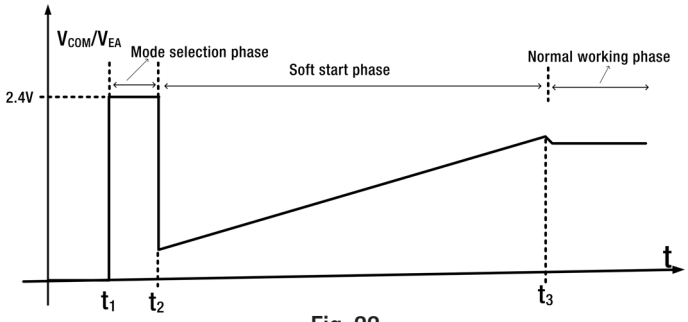


Fig. 22

Normal Operation State

Without triggering any protection logic, the output voltage of the converter is established during startup, forming a closed-loop feedback at time t_3 as shown in Figure 22. At this point, the soft-start phase ends, and the system transitions into the normal closed-loop regulation state. Depending on the output load conditions of the converter, the control voltage V_{COM} or V_{EA} rises to different levels by the end of soft start t_3 and stabilizes accordingly. The system may then operate either at the fixed oscillator frequency F_{OSC}, or in an analog frequency reduction mode (analog down-conversion), based on load demands and loop conditions.

Output Overload, SCP, OLP

Common abnormal conditions in a converter include the output load exceeding the design limit, output short circuits, poor solder joints (virtual soldering), or component failures. These issues can cause the feedback loop to become open, leading to unstable or unsafe operation. RVPW015 is equipped with comprehensive protection mechanisms to handle such faults, with the timing sequence illustrated in Figure 23. All three fault types can result in the duty cycle modulation voltage-either V_{COM} or V_{EA}-rising excessively and exceeding the open-loop protection threshold of 4.5V. If the chip's VDD voltage is below 5.3V, this threshold becomes VDD–0.8V. Once such a condition is detected, the chip begins timing. If the fault occurs during the soft start phase, timing starts from the first switching pulse. If the overvoltage condition persists for more than 55ms without interruption (any interruption resets the timer), the controller enters protection mode. After entering protection, the system pauses operation for 1.4 seconds before automatically attempting to restart. Additionally, if VDD exceeds 10V during this period, overvoltage protection is immediately triggered, causing the system to enter protection mode ahead of the 55ms timeout. By observing the duration of DRN output pulses and the V_{DD} voltage just prior to protection, designers can accurately determine which protection mechanism was activated. This diagnostic capability is especially helpful for identifying the root cause of converter failures during development and troubleshooting.

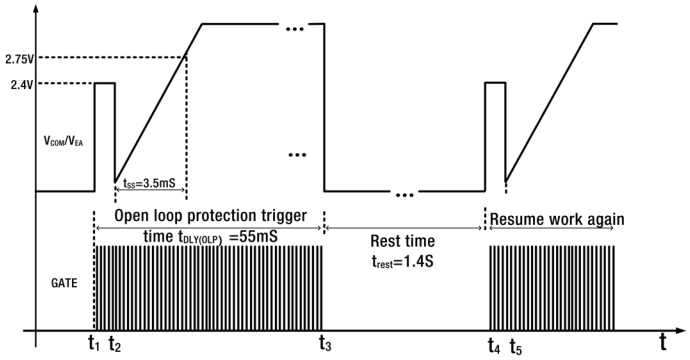


Fig. 23

APPLICATION CASES

Application Information

Startup Circuit

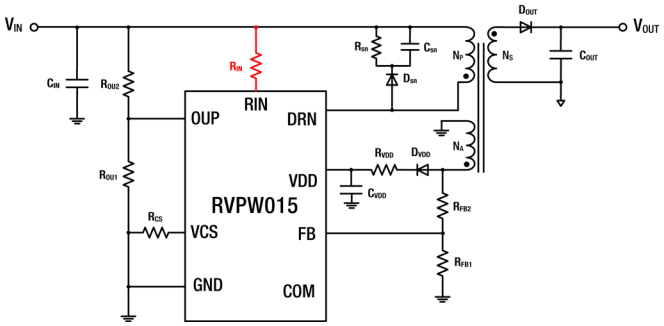


Fig. 24

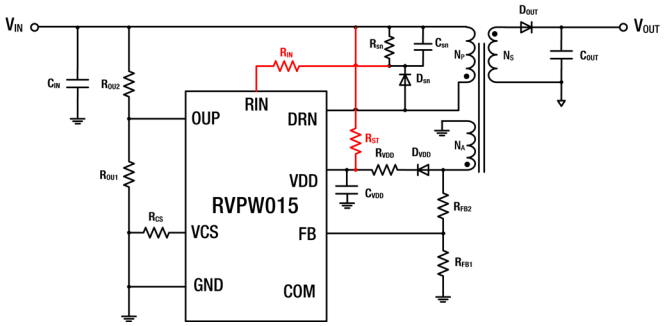


Fig. 25

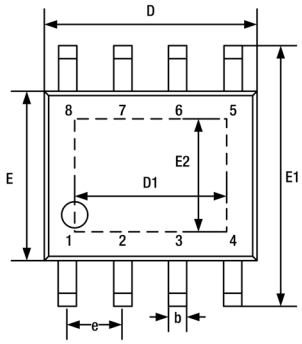
For applications where the minimum input voltage V_{IN} is greater than 6V, the startup circuit shown in Figure 24 should be used. In this configuration, resistor R_{IN} supplies bias current to the internal startup MOSFET, which in turn sources startup current from the DRN pin to the VDD pin. Once the converter's output voltage V_{OUT} is established, power is supplied to the chip via the auxiliary winding N_A. For applications where the minimum V_{IN} is less than 6V, the startup circuit shown in Figure 25 is recommended. In this case, R_{IN} should be connected to the RCD snubber (absorption) circuit, and an additional resistor R_{ST} must be connected between V_{IN} and VDD to ensure proper startup. The recommended value for R_{ST} is:

$$\frac{V_{IN(MAX)} - 9.5V}{4.5mA} < R_{ST} < \frac{V_{IN(MIN)} - 3.5V}{100\mu A}$$

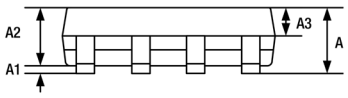
Among them, $V_{IN(MIN)}$ is the minimum input voltage, $V_{IN(MAX)}$ is the maximum input voltage, 3.5V is the upper limit of V_{DD} startup voltage $V_{DD(ON)}$, 100uA is the upper limit of $I_{VDD(ON)}$, 9.5V is the lower limit of $V_{DD(OVP)}$, and 4.5mA is the lower limit of $I_{VDD(OVP)}$.

PACKAGING INFORMATION

ESOP8

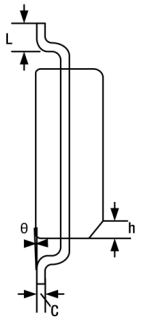


Package top view

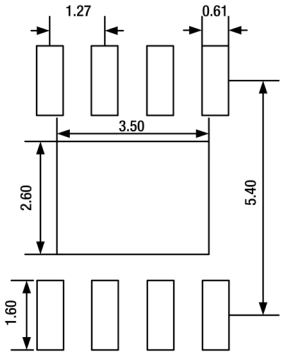


Package front view

DIMENSIONTABLE			
SYMBOL	MILLIMETER		
	MINIMUM	NOMINAL	MAXIMUM
A	1.5	1.6	1.7
A1	0.04	---	0.12
A2	1.35	1.45	1.55
A3	0.65	0.7	0.75
b	0.35	---	0.5
c	0.19	---	0.25
D	4.8	4.9	5
D1	3.2	3.3	3.4
E	3.8	3.9	4
E1	5.8	6	6.2
E2	2.3	2.4	2.5
e	1.27 BSC		
h	0.3	---	0.5
L	0.5	---	0.8
θ	0°	---	8°



Package side view



Recommended solder pads

ORDER INFORMATION

Device	Package Type	PIN	Packaging Method	QTY	Marking Code*	MSL
RVPW015-FJ2-R	ESOP8	8	Tape and Reel	4000	RVPW015	MSL-3

*Marking Code :
RVPW015—— Product Code