RVPW014 Current Mode PWM Controller

4-50VIN/90V/0.1Ω POWER MOSFET

FEATURES

- Suitable for PSR and SSR flyback/Boost/Buck
- PSR Feedback Minimum Sampling Time as Low as 0.4us
- CCM and DCM Modes are Compatible
- Integrated 90V/0.1Ω LDMOS
- Integrated Lossless Current Sampling
- Programmable Peak Current
- Programmable Power MOSFET Driving Speed
- Programmable Frequency Jitter Function
- Programmable Input Undervoltage and Overvoltage Protection
- Overcurrent Protection, Short Circuit Protection, and Over Temperature Protection
- Linearly Decrease of the Operating Frequency to Optimize Efficiency under Light-load Conditions
- Internal Feedforward Compensation Function
- Internal Soft Start and Slope Compensation
- Internal PSR Loop Control in CCM/DCM Mode
- Direct Optocoupler Interface
- Internal Loop Compensation and Output Diode Voltage Drop Temperature Compensation
- ESOP8 Strong Heat Dissipation Packaging

APPLICATIONS

- DCM/CCM Flyback Converter
- Industrial Power Conversion
- BMS Auxiliary Power Supplies
- POE Power Supplies
- Isolation Communication Power Supplies

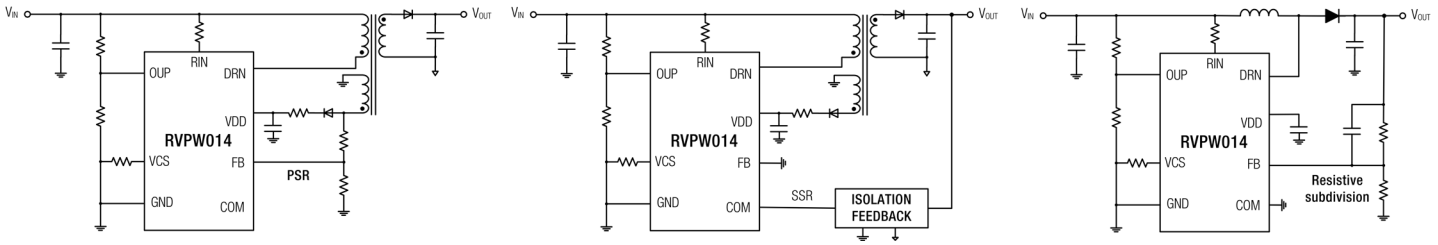
DESCRIPTION

RVPW014 is a highly integrated power control chip designed for multiple power topologies, including Flyback, Boost, and Buck, and supports various output voltage feedback methods such as SSR (Secondary-Side Regulation), PSR (Primary-Side Regulation), and resistive voltage division. The chip supports PSR feedback at switching frequencies of several hundred kHz. Its internal output voltage sampling circuit functions in both CCM (Continuous Conduction Mode) and DCM (Discontinuous Conduction Mode), with a sampling time requirement as short as 400ns. A built-in loop compensation circuit featuring fast dynamic response ensures excellent system stability and transient performance for switching power supplies. RVPW014 integrates multiple control features while requiring only simple external components, allowing flexible design based on application needs. It supports three programmable functions-startup timing, feedforward compensation, and internal power MOSFET shutdown rate-through a single external resistor. Peak current of the power MOSFET can also be set via a resistor, enabling “lossless” current sensing. Input undervoltage and overvoltage protection thresholds can be configured simultaneously using just two resistors. A frequency jitter function is available by connecting a capacitor between the FB pin and GND. The jitter period is programmable via the capacitor value. If the FB pin is directly connected to GND, the frequency jitter function is disabled. RVPW014 includes comprehensive protection features: overcurrent protection (OCP), overload protection (OLP), output short-circuit protection (SCP), output overvoltage protection (OVP), and over-temperature protection (OTP). The chip supports automatic recovery once the fault condition is cleared, thereby enhancing the overall reliability of the power supply system.

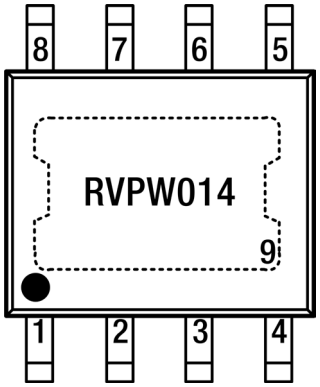
Device information

Part Number	Package	Weight(mg)	Dimension	QTY
RVPW014	ESOP8	77.00	5.0mm x 6.0mm	4000

SIMPLIFIED SCHEMATIC



PIN CONFIGURATION AND FUNCTIONS



Name	ESOP8 PIN No.	Type	Description
COM	1	I	In SSR operating mode, the optocoupler feedback pin controls both peak current and switching frequency through the voltage applied to it. This pin includes an internally integrated RC compensation circuit, allowing direct connection to an optocoupler without the need for additional external components.
VDD	2	I	Chip's power supply input, VDD, provides power to the internal control circuitry through an integrated low-dropout regulator (LDO), which generates an internal supply voltage, V_{CC}. The LDO operates in the linear region with a typical V_{CC} output of 5.3V, enters the dropout region when VDD falls close to V_{CC}, maintaining a typical dropout voltage of approximately 0.3V. VDD also features an internal voltage clamp with a clamping threshold of approximately 10V. If the current drawn by the clamp exceeds 5.3mA, the chip disables the internal power MOSFET and enters a self-recovery protection mode to ensure safe operation.
VCS	3	I	Peak Current Threshold Setting Pin. Connect a resistor (typically in the tens of kΩ range) from this pin to GND to set the maximum and minimum peak current thresholds in PSR mode. This configuration enables internal lossless current sensing.
GND	4	P	Ground Reference (GND). This pin serves as the signal ground for the internal control logic and also functions as the source terminal of the internal LDMOS device.
DRN	5	O	The drain of the internal LDMOS.
RIN	6	I	Connecting an external resistor to the VIN pin enables startup control, adjustment of the power MOSFET shutdown speed, and implementation of feedforward compensation.
OUP	7	I	Input Overvoltage/Undervoltage Protection (Multiplexed Pin). This pin is used for both input undervoltage and overvoltage protection. Undervoltage protection threshold and recovery point can be configured by adjusting the resistor ratio of an external voltage divider. Overvoltage protection threshold is determined by the absolute values of the voltage divider resistors.
FB	8	I	Output Voltage Feedback Pin (FB). This pin is used to sample the output voltage of the switching power supply. Feedback can be obtained either through an auxiliary winding for isolated regulation, or via a resistor voltage divider for non-isolated topologies such as Flyback, Buck, or Boost. The sampled voltage is processed by an internal error amplifier to regulate the duty cycle of the power MOSFET, ensuring stable output voltage. In SSR mode, connecting a capacitor from the FB pin to GND enables the frequency jitter function. To disable frequency jitter, connect the FB pin directly to GND.
EP	9	P	Exposed Pad (EP). Internally connected to GND. For optimal thermal performance, the EP should be soldered to a large ground plane. Note that the exposed pad is intended for heat dissipation only and is not used as an electrical signal connection point.

SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage Range of RIN to GND	V_{RIN}	-0.3	35	V
VDD to GND	V_{DD}	-0.3	13	V
DRN to GND	V_{DRN}	-1.3	90	V
FB to GND	V_{FB}	-0.75	6	V
Peak Current of FB to GND	$I_{FB(PEAK)}$		-2.5	mA
Other Pins to GND	V_{COM}, V_{OUP}, V_{CS}	-0.3	6	V
Maximum Operating Junction Temperature	T_{JMAX}		150	°C

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model HBM, per ESDA/JEDEC JS-001-2023; (Zap 1 pulse, Interval :>=0.1S)	±2000	V
		Charged device model CDM, per ESDA/JEDEC JS-002-2022	±1000	V

Thermal Resistance

Packaging	θ_{JA}	Ψ_{JT}	UNIT
ESOP8	51.9	6.5	°C/W

Note: The measurements were made on a test plate with a thickness of 1oz and an area of 7.62 x 11.43CM

Recommended Operatings Conditions

		MIN	NOM	MAX	UNIT
Power MOSFET Drain Voltage	V_{DRN}			81	V
VDD Input Voltage	V_{DD}	4		10	V
VCS External Resistor	R_{CS}	12			kΩ
RIN External Resistor	R_{IN}			1	MΩ
FB Current	I_{FB}	-2			mA
Ambient Temperature	T_A	-40		125	°C

Electrical Characteristics

Unless otherwise specified, the following parameters were measured under the condition of V_{DD}=7V and temperature T=25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
$V_{DD(ON)}$	VDD turn on threshold	V_{DD} rising	3.1	3.3	3.5	V
$V_{DD(OFF)}$	VDD turn off threshold	V_{DD} falling	2.8	3.0	3.2	V
$I_{VDD(ON)}$	VDD turn on current	V_{DD} rising		61	100	uA
$I_{VDD(OP)}$	Operating current at full load in SSR mode	Connect COM to 6.8kΩ to GND, V_{FB}=0V	1.9	2.5	3.3	mA
$I_{VDD(UVP)}$	Operating current under input voltage	OUP=0V		143	200	uA
$V_{DD(DMAX)}$	MOSFET for starting up supply voltage@D_{MAX}	F_{DRN}=330kHz, 80% duty cycle	3.3	3.8	5.0	V
$V_{BV(DIODE)}$	Break voltage of anti reflow diode		37			V
$V_{DD(OVP)}$	VDD overvoltage shutdown threshold	V_{DD} rising	9.5	10	10.8	V
$I_{VDD(OVP)}$	VDD absorbs current during overvoltage protection	V_{DD}= $V_{DD(OVP)}$	4.5	5.3	6.5	mA
RIN						
V_{ZB}	MOSFET for starting up bias voltage	I_{RIN}=1uA	6.0	6.9	8.0	V
$R_{IN(IN)}$	Input resistance			100		kΩ
VCS						
$V_{CS(MAX)}$	Maximum threshold voltage		1.85	2.00	2.15	V
$V_{CS(MIN)}$	Minimum threshold voltage	PSR mode	225	250	275	mV
		SSR mode	80	100	120	mV
k_{CS}	Proportional coefficient between peak current of power MOSFET and VCS current		27200	32000	36800	A/A
$D_{35\%}$	Initial duty cycle of adding slope compensation			35		%
OUP						
$V_{OUP(ON)}$	Undervoltage protection turn on voltage		1.9	2.0	2.1	V
$V_{OUP(OFF)}$	Undervoltage protection turn off voltage		1.67	1.75	1.83	V
$V_{OUP(OC)}$	Input overcurrent protection clamp voltage	I_{OUP}=50uA injected into OUP pin	2.1	2.2	2.4	V
$I_{OUP(OFF)}$	Input overcurrent protection comparison current	I_{OUP} gradually increasing	92	100	108	uA
$I_{OUP(ON)}$	Input overcurrent protection recovery comparison current	I_{OUP} gradually decreasing	83	90	97	uA
FB						
$V_{REF(REG)}$	Reference voltage of EA		1.97	2.00	2.03	V
A_V	Low frequency gain of EA			1400		V/V
$V_{REF\_H(FJ)}$	High value comparison voltage of jitter frequency	Connect COM to 6.8kΩ to GND, connect FB to 22nF to GND	2.85	3.0	3.15	V
$V_{REF\_L(FJ)}$	Low value comparison voltage of jitter frequency		0.70	0.75	0.80	V
$T_{D(SAMP)}$	Delay time of sampling			252	350	nS
K_{VTC}	The temperature coefficient of temperature compensation voltage			3.5		mV/°C
I_{FB}	Pin output current	When the FB pin is used as a feedback voltage		-40		nA
		When using the frequency jitter function, the charging and discharging current		±24		uA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
COM						
$V_{COM(OPEN)}$	Open loop voltage		5.0	5.3	5.6	V
$V_{COM(OLP)}$	Threshold voltage of OLP	VDD≥5.3V	4.0	4.5	5.0	V
		VDD<5.3V		VDD - 0.8		V
I_{COM}	Maximum output current of COM	V_{COM}=0V	1.06	1.3	1.59	mA
$V_{COM(IMAX)}$	Pin voltage at maximum peak current	COM rises until V_{CS}=$V_{CS(MAX)}$	2.60	2.75	2.90	V
t_{SS}	Soft start time	V_{COM} rising	2.6	3.6	4.6	mS
DRN						
$R_{DS(ON)}$	MOSFET on-state resistance	I_{DS}=2A, T=25°C		100		mΩ
		I_{DS}=2A, T=125°C		163		mΩ
I_{SCP}	The current of Short-circuit protection		6.5	9.5	12.5	A
f_{OSC}	Maximum operating frequency	Frequency without simulated downsampling	300	330	360	kHz
f_{MIN}	Minimum operating frequency		6	9	12	kHz
D_{MAX}	Maximum duty cycle		75	80	85	%
$t_{ON(MIN)}$	Minimum conduction time	VCS suspended, drain connected to a 120Ω pull-up resistor		250		nS
$t_{ON(MAX)}$	Maximum conduction time		2.15	2.4	2.65	uS
OTHER PROTECTIVE FUNCTIONS						
T_{SHDN}	Over temperature protection threshold		148	163	178	°C
$T_{SHDN(HYS)}$	Over temperature protection hysteresis			18		°C
$t_{DLY(OLP)}$	OLP trigger time	From V_{COM}>$V_{COM(OLP)}$ to entering protection		55		mS
t_{rest}	Rest time after self recovery protection			730		mS

Typical Characteristics

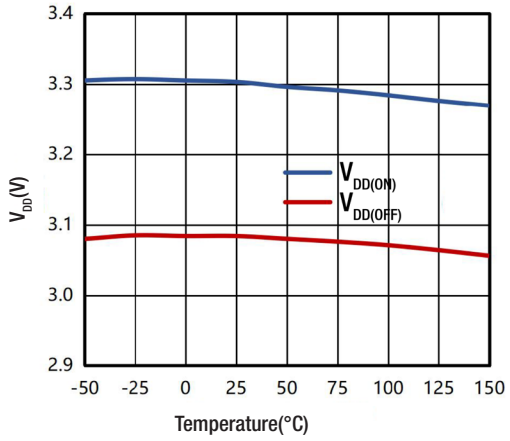


Fig. 1 $V_{DD(ON)}$ and $V_{DD(OFF)}$ vs Temperature

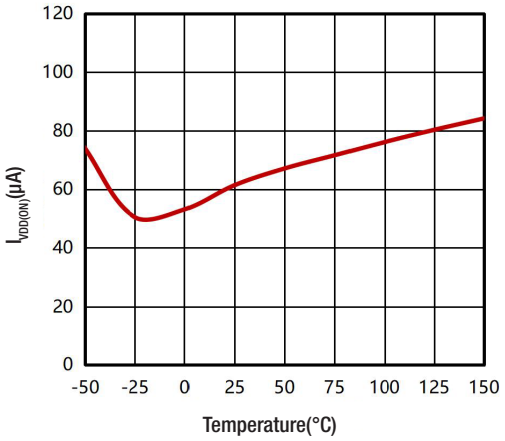


Fig. 2 $I_{VDD(ON)}$ vs Temperature

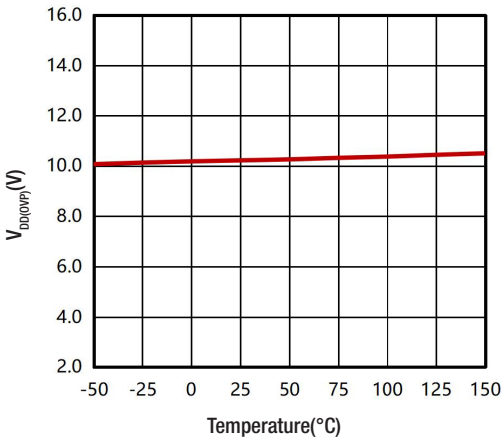


Fig. 3 $V_{DD(OVP)}$ vs Temperature

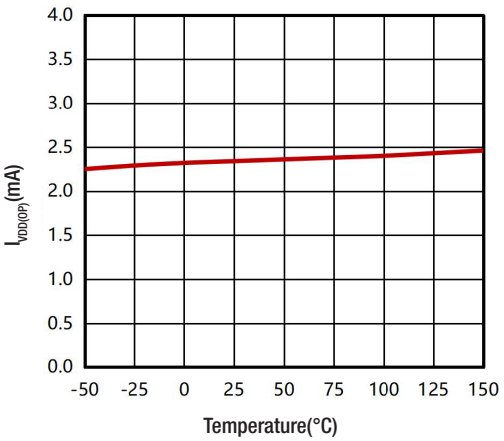


Fig. 4 $I_{VDD(OP)}$ vs Temperature

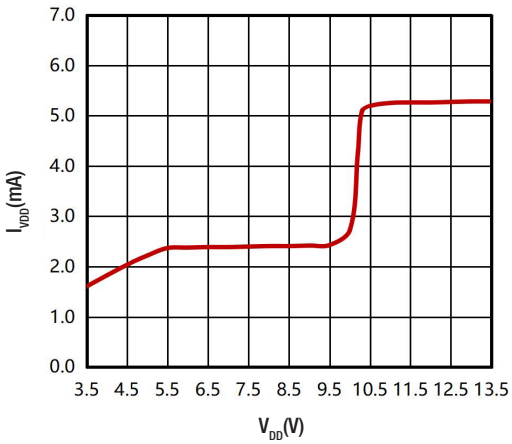


Fig. 5 I_{VDD} vs V_{DD}

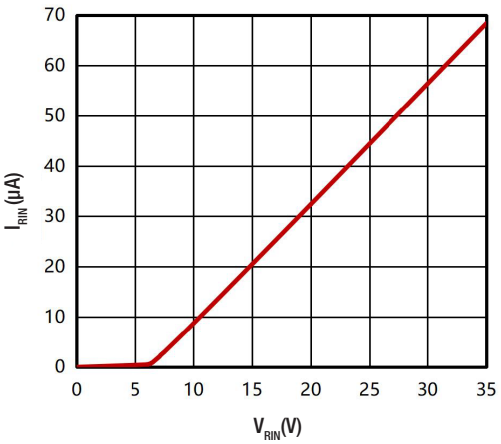


Fig. 6 I_{RIN} vs V_{RIN}

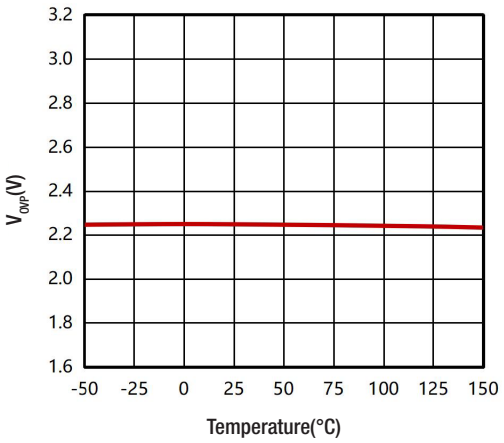


Fig. 7 $V_{OUP(OC)}$ vs Temperature

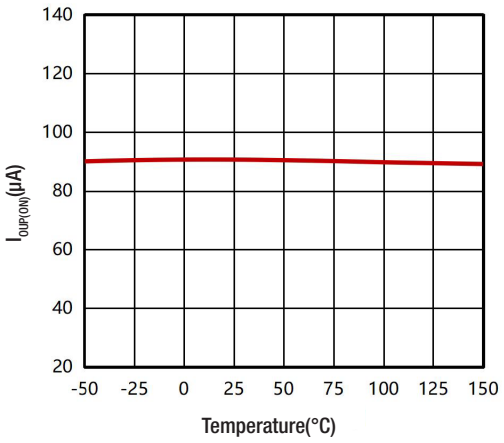


Fig. 8 $I_{OUP(ON)}$ vs Temperature

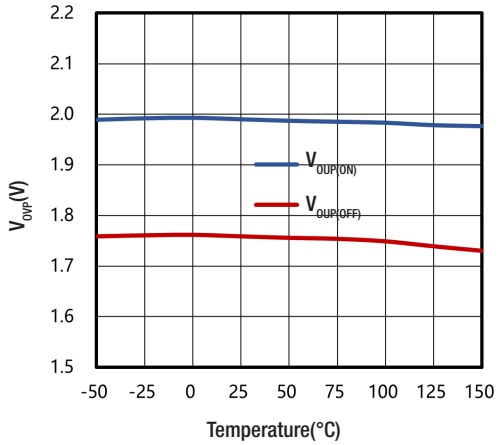


Fig. 9 $V_{OUP(ON)}$ and $V_{OUP(OFF)}$ vs Temperature

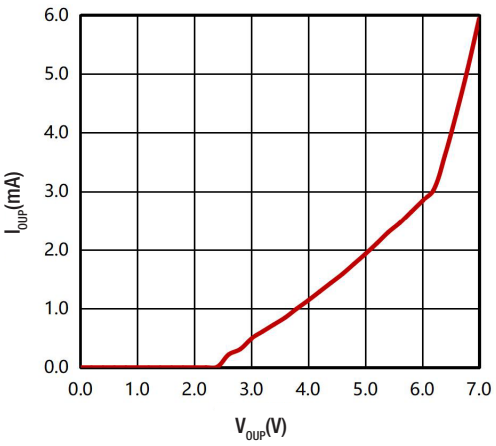


Fig. 10 I_{OUP} vs V_{OUP}

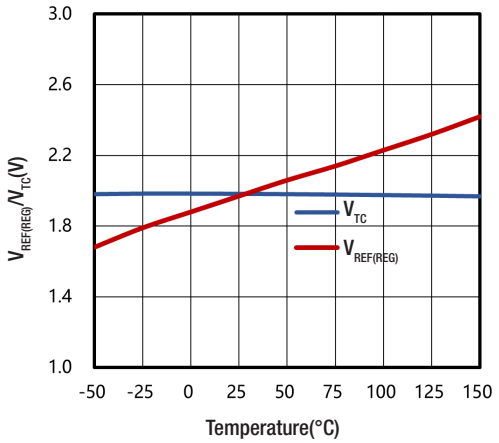


Fig. 11 $V_{REF(REG)}/V_{TC}$ vs Temperature

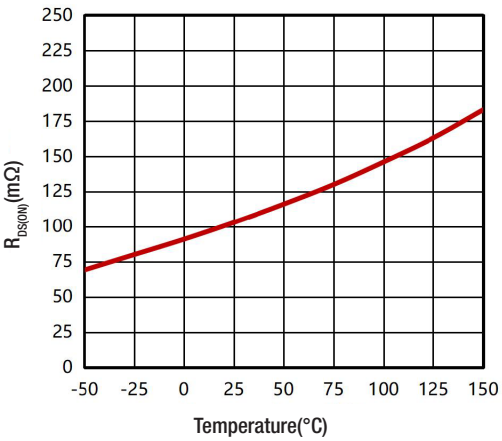


Fig. 12 $R_{DS(ON)}$ vs Temperature

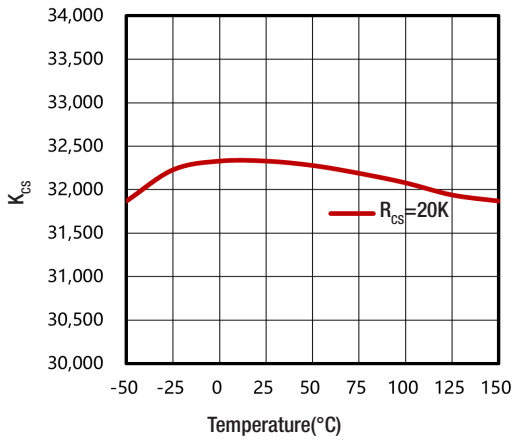


Fig. 13 K_{CS} vs Temperature

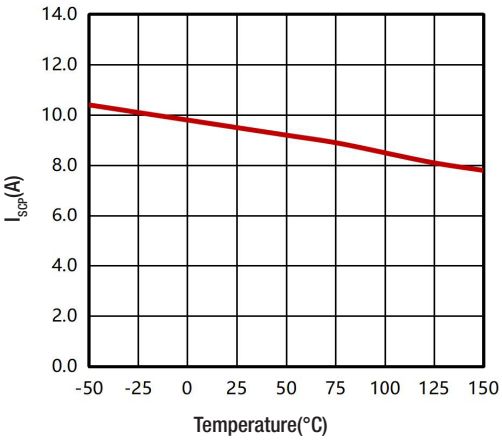


Fig. 14 I_{SCP} vs Temperature

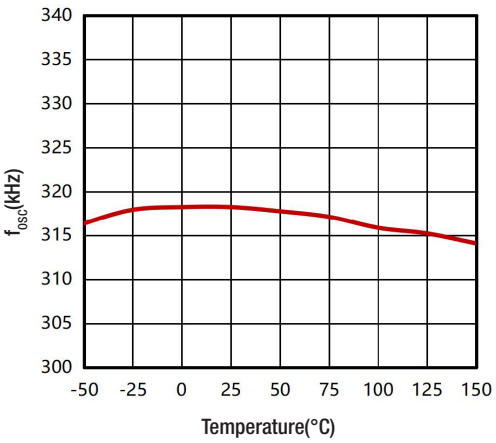


Fig. 15 f_{OSC} vs Temperature

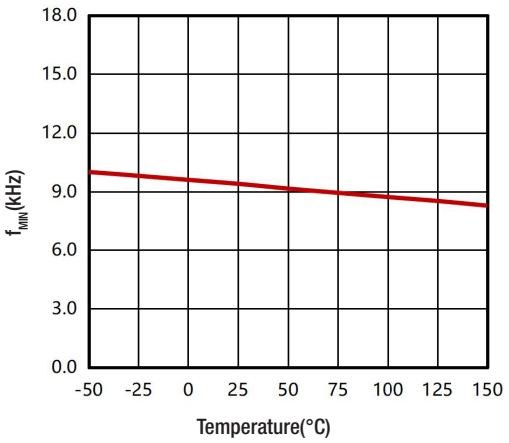


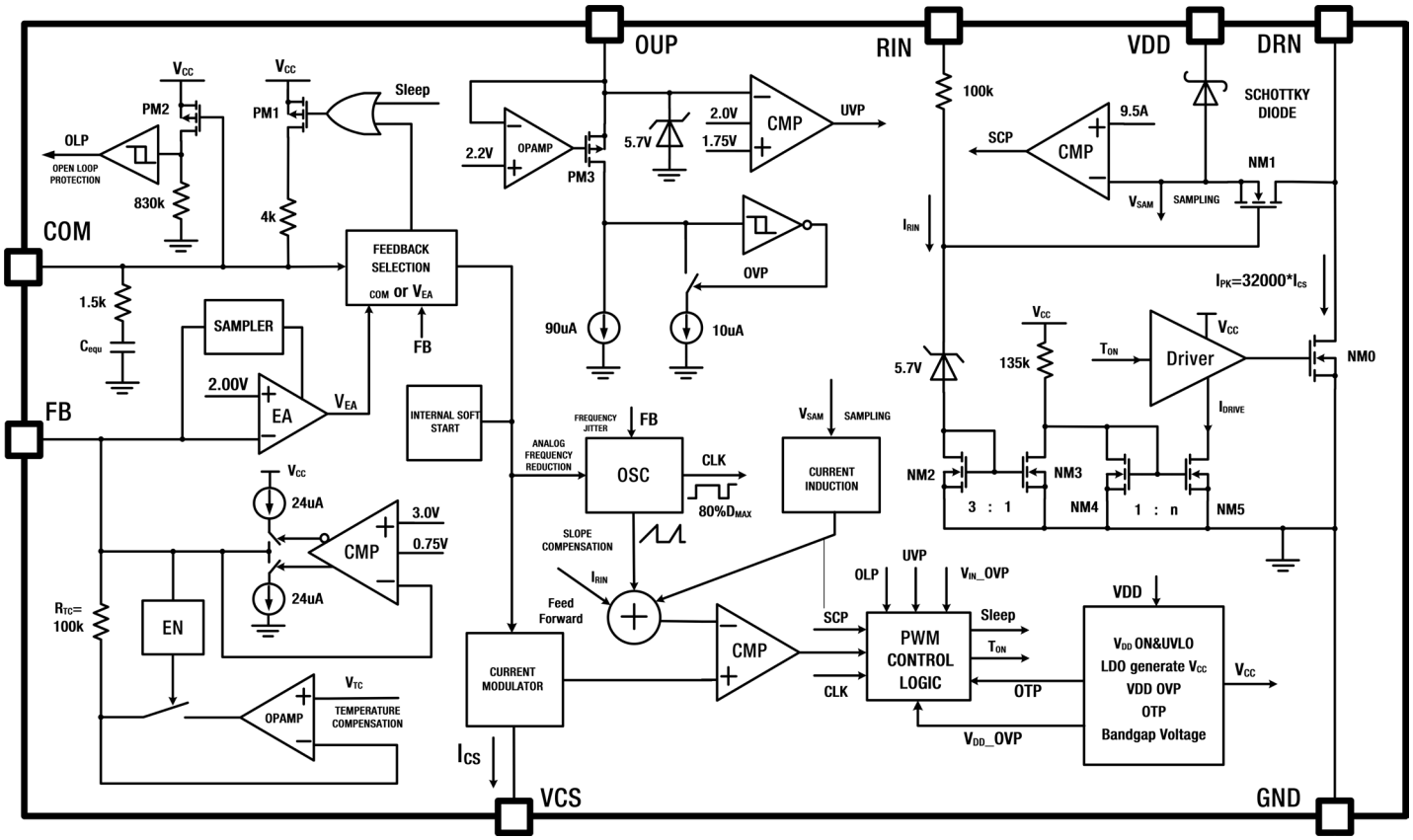
Fig. 16 f_{MIN} vs Temperature

FUNCTIONS AND PRINCIPLES

Overview

RVPW014-Integrated Current Mode PWM Controller with Internal Power MOSFET. RVPW014 is a current-mode PWM controller that integrates control circuitry and a power MOSFET on a single chip using advanced BCD technology. It is suitable for a wide range of switching power supply topologies-including Flyback, Buck, and Boost-with output power up to 15W. The device features two feedback pins, COM and FB, supporting both isolated and non-isolated regulation methods. For isolated applications requiring high output voltage accuracy, the COM pin supports secondary-side regulation (SSR) using an optocoupler and reference components like the TL431. This configuration provides precise output voltage control for Flyback converters. For cost-sensitive applications where high voltage accuracy is not critical, the primary-side regulation (PSR) method can be used. In this case, the FB pin receives feedback from the auxiliary winding of the Flyback transformer, eliminating the need for an optocoupler. In non-isolated topologies such as Buck and Boost, the output voltage can be directly sampled and fed back to the FB pin via a resistor divider network to maintain output voltage stability. The RVPW014 supports both CCM (Continuous Conduction Mode) and DCM (Discontinuous Conduction Mode) operation, enabling power supply miniaturization and high efficiency. Its versatility and wide input voltage compatibility make it ideal for applications such as IGBT-based motor drives, industrial automation systems, medical instruments, and other environments with demanding power requirements.

Functional Block Diagram



Feature Description

Function and Resistance Design of External Resistor R_{IN}

As shown in Figure 17, a resistor R_{IN} is connected between the R_{IN} pin of the RVPW014 and the input voltage V_{IN} of the converter. This resistor serves three main functions: it provides bias voltage for initiating the internal startup MOSFET NM1, programs the turn-off speed of the internal power MOSFET NM0, and enables feedforward compensation based on input voltage.

Startup and Power Supply: R_{IN} resistor supplies bias current to a 5.7V Zener diode and to NM2, which is connected between the gate and source terminals. The sum of the Zener breakdown voltage and the gate-to-source threshold of NM2 is approximately 6.9V, which provides the necessary bias voltage to activate NM1. Once biased, NM1 conducts startup current, which flows from the DRN pin (the drain of NM0) through NM1 and a Schottky diode to charge the VDD capacitor. After the converter's output voltage is established, it is recommended to power the VDD pin using an auxiliary winding. This avoids continuous use of the internal startup circuit, which incurs significant power loss. For reliable shutdown of the startup path, the VDD voltage should be maintained above 6V during normal operation. Additionally, VDD pin integrates both a voltage clamp and overvoltage protection. The internal clamp activates at approximately 10V. If the current drawn by the clamp exceeds 5mA, the chip enters an overvoltage protection mode and disables the internal MOSFET. In flyback converter applications, this overvoltage protection feature can also serve as output overvoltage protection, by leveraging the proportional relationship between the voltage of the auxiliary winding and the output winding.

Switching Speed of NM0: The switching speed of the internal power MOSFET NM0 is controlled by the input current I_{RIN}, which is drawn through the R_{IN} resistor. This current is internally processed to generate the gate driving current I_{DRIVE}, which in turn determines the turn-off behavior of NM0. The relationship between I_{RIN} and I_{DRIVE} is defined as follows:

$$\frac{I_{DRIVE}}{n} = \frac{V_{CC} - V_{GS4}}{135k\Omega} - \frac{1}{3} \times \frac{V_{IN} - 5.7V - V_{GS2}}{R_{IN} + 100k\Omega}$$

In the equation described above, V_{CC}=5.3V and $V_{GS2} \approx V_{GS4} \approx 1.2V$. When R_{IN}=330kΩ, and the equation yields zero, I_{DRIVE}=0 occurs at an input voltage of V_{IN}= 46V. At this point, the gate driver circuit turns the internal power MOSFET (NM0) on and off using only its inherent driving capability, resulting in the slowest turn-off speed. When I_{DRIVE}>0, the shutdown speed of NM0 increases accordingly. From the equation, two key relationships can be observed: By adjusting the R_{IN} value, the shutdown speed of NM0 can be programmed. A larger R_{IN} results in a faster turn-off speed. As the input voltage increases, I_{DRIVE} decreases, causing a slower NM0 turn-off. This behavior helps suppress voltage spikes caused by leakage inductance under high input voltage conditions.

Feedforward Compensation Function: The current through NM2 (I_{RIN}) is proportionally mirrored and used as a feedforward compensation current. This current is superimposed with both the power MOSFET NM0 sampling current and the slope compensation current, forming the input to the PWM comparator. Since the feedforward current increases with input voltage, it helps minimize variation in the overcurrent protection point at different input levels, compensating for delays in both the PWM comparator and gate driver circuitry.

R_{IN} Resistor Design Guidelines: An internal 100kΩ resistor is connected in series with the R_{IN} pin. This serves two purposes: first, it absorbs part of the input voltage to ensure adequate voltage withstand capability, even when using ultra-compact external resistors. Second, for low input voltage applications, it may be possible to omit the external R_{IN} resistor altogether. While the R_{IN} value is not critical for the startup function-i.e., biasing the startup MOSFET NM1-it directly impacts both the turn-off speed of NM0 and the feedforward compensation characteristics. Therefore, R_{IN} should be selected as a tradeoff between these two performance factors. A typical value falls in the range of several hundred kilohms, depending on application requirements.

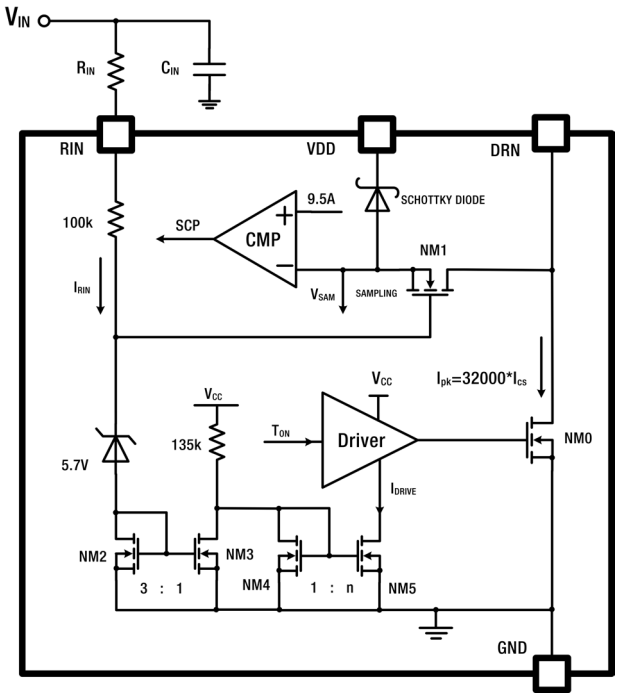


Fig. 17 Startup and shutdown speed

Input Over/Under Voltage Protection

As shown in figure 18, the input overvoltage and undervoltage protection functions of the RVPW014 are implemented through a single pin, OUP. The threshold voltages for both protections can be programmed based on application requirements. The operating principle is as follows: When the voltage at the OUP pin is less than 2.2V, the pin draws no current. Under this condition, the turn-on and turn-off thresholds for input undervoltage protection V_{IN} can be easily calculated using the following formulas:

$$V_{INON(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2V$$

$$V_{INOFF(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 1.75V$$

When the voltage at the OUP pin exceeds 2.2V, the pin begins to draw current and maintains this voltage level until the current exceeds 100μA. At this point, the condition is recognized as an OUP input overcurrent, triggering the chip to stop switching the power MOSFET NM0 and enter a protection state. As the input voltage decreases and the current drawn by the OUP pin falls below 90μA, the chip automatically exits the protection mode and resumes normal operation. The input overvoltage protection threshold and recovery voltage can be calculated using the following formulas:

$$V_{INOFF(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2.2V + 100\mu A \times R_{OU2}$$

$$V_{INON(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2.2V + 90\mu A \times R_{OU2}$$

When designing the resistance values of R_{OU1} and R_{OU2}, a more practical formula can be obtained to quickly determine the resistance:

$$R_{OU2} = \frac{V_{INOFF(OVP)} - 1.1 \times V_{INON(UVP)}}{100\mu A}$$

As long as the operating range of the input voltage of the converter is determined, R_{OU2} can be calculated, and then combined with the undervoltage protection formula, R_{OU1} can be calculated.

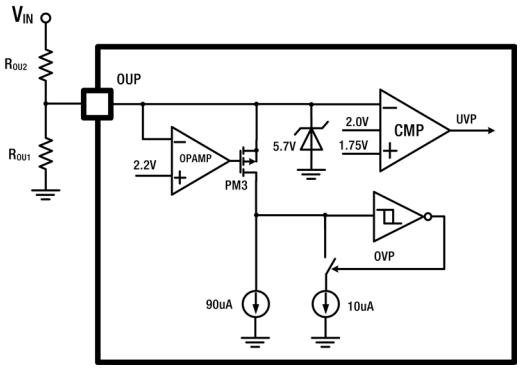


Fig. 18 Input Over/Under Voltage Protection

Mode Selection of Multiple Voltage Feedback Methods

RVPW014 supports multiple feedback modes, including secondary-side regulation (SSR) using optocoupler-based isolation, primary-side regulation (PSR) via transformer auxiliary windings, and direct sampling through a resistive voltage divider. In SSR mode, the closed-loop feedback signal is input through the COM pin, while in PSR and resistive divider modes, the feedback is sensed through the FB pin. The appropriate operating mode is automatically selected based on the external circuit configuration during the first 12 switching cycles after power-up or restart from a protection event. If the COM pin is used for feedback, its voltage directly serves as the modulation reference for PWM duty cycle comparison. Conversely, if the FB pin is selected, the V_{EA} output of the internal error amplifier is used as the duty cycle modulation reference for PWM comparison. The required pin configurations for each feedback method are as follows:

Feedback method	COM pin	FB pin
Optocoupler feedback SSR	Connect to optocoupler	If frequency jitter is required, connect the capacitor to GND; otherwise, connect to GND
Winding feedback PSR	Float	Auxiliary winding resistance voltage divider terminal
Direct sampling of resistive subdivision	Connect to GND	Resistance voltage divider terminal of the converter output

PWM and PFM Control

Current Sampling: RVPW014 performs current sampling by detecting the conduction voltage drop across the internal power MOSFET NM0. This voltage is measured at the source of the startup MOSFET NM1 and replicated via an internal operational amplifier. The signal is then mirrored to a sampling MOSFET a device of the same type as NM0 but with higher internal resistance. As a result, an induced current proportional to the peak current (I_{PK}) of NM0 is generated in the sampling MOSFET, allowing for lossless current sensing.

Current modulator: The pulse-width modulation voltage, either V_{COM} (in SSR mode) or V_{EA} (in PSR mode), produces a corresponding modulation current across the external resistor connected to the V_{CS} pin. As shown in Figure 19, there is a defined relationship between V_{COM}/V_{EA} and V_{CS}. As V_{COM} or V_{EA} increases, V_{CS} also increases, generating a proportional current that modulates the peak current of NM0, thereby regulating the converter's output voltage. When V_{COM}/V_{EA}>2.75V, V_{CS} reaches its maximum value $V_{CS(MAX)}$, which limits the maximum peak current of NM0. The minimum voltage of VCS depends on the feedback mode: In SSR mode, $V_{CS(MIN)}$=100mV. In PSR mode, $V_{CS(MIN)}$=250mV. A higher $V_{CS(MIN)}$ (as in PSR) allows FB for a longer demagnetization time, improving sampling accuracy of the output voltage. However, it also increases the minimum energy per switching cycle, which may require larger dummy loads to prevent output voltage overshoot under no-load conditions.

PWM Control: Modulation current generated from V_{CS} serves as the positive input to the internal PWM comparator. The negative input is the sum of three components: The induced current from the sampling MOSFET. Slope compensation current. Feedforward compensation current. Comparator outputs a pulse-width signal to control NM0, ensuring the output voltage of the converter remains regulated. The maximum output duty cycle is limited to 80%. To prevent subharmonic oscillation when the duty cycle exceeds 50%, RVPW014 integrates an internal ramp compensation circuit. Ramp current is derived from the oscillator's ramp waveform. To reduce the impact of ramp compensation on low-input-voltage performance, the ramp compensation current is only active when the duty cycle exceeds 35%. Below this threshold, slope current compensation is disabled. When the duty cycle reaches its maximum of 80%, the ramp compensation current also reaches its maximum value.

PFM Control (Frequency Reduction at Light Load): To improve efficiency at light load and reduce no-load power consumption, the RVPW014 includes a frequency reduction function based on the load level. As load decreases, the modulation voltage (V_{COM} or V_{EA}) also declines. When the load drops to approximately 30% of the converter's maximum rated power, the operating frequency begins to decrease in proportion to V_{COM}/V_{EA}. The minimum switching frequency is f_{MIN}=9kHz. The relationship between switching frequency and V_{COM}/V_{EA} is illustrated by the red solid line in Figure 19.

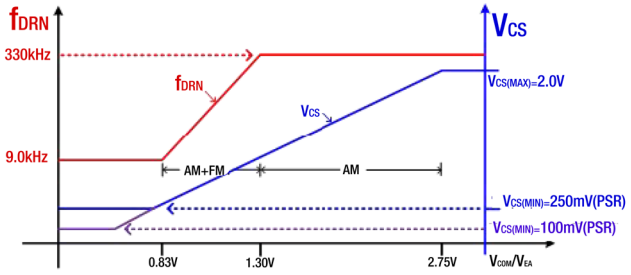


Fig. 19 Variation Curves of Switching Frequency and Peak Current Modulation with V_{COM} and V_{EA}

Programmable Frequency Jitter Function

In SSR mode, the COM pin functions as the loop feedback port, while the FB pin supports a programmable frequency jitter function. The resonant voltage at the FB pin periodically varies in frequency, with the maximum amplitude of the frequency jitter fixed at ±6%. The term "programmable" refers to the following configurations: (1) Connecting FB directly to GND disables the frequency jitter function; (2) Connecting an external capacitor (C_{FJ}) from FB to GND enables the frequency jitter function. The period of the frequency variation is determined by the value of the C_{FJ} capacitor.

$$T_{FJ} = \frac{C_{FJ}}{22nF} \times 4.2mS, \text{suggest a } C_{FJ} \text{ value of } 22nF$$

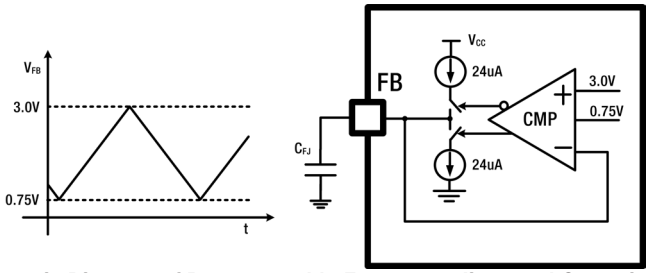


Fig. 20 Schematic Diagram of Programmable Frequency Jitter and Operating Waveform

Peak Current Setting of Power MOSFET

The peak current of the power MOSFET (NM0) in the RVPW014 is regulated by a current modulator, which adjusts the current I_{CS} based on the voltage at the VCS[3] pin and the external resistor R_{CS}. The drain current of the power MOSFET is 32,000 times the value of I_{CS}.

The value of Rcs can be calculated using the following formula:

$$R_{CS} = 32000 \times \frac{V_{CS(MAX)}}{I_{PK}}$$

Among them: $V_{CS(MAX)}$ is the maximum threshold voltage of the VCS pin, with a typical value of 2V;
I_{PK} is the maximum peak current of the primary winding of the flyback converter.

FB Pin PSR Feedback Voltage Sampling

RVPW014 monitors the output voltage of the switching power supply via the auxiliary winding of the transformer. A sampling resistor connected to the auxiliary winding feeds the signal to the FB pin. During the transformer's demagnetization phase, the sampled voltage serves as the negative input to the error amplifier (EA). This voltage is differentially amplified against the internal reference voltage $V_{REF(REG)}$=2V to generate the duty cycle control voltage V_{EA}, which in turn modulates the converter's duty cycle, as illustrated in Figure 21. The corresponding auxiliary winding voltage waveform is shown in Figure 22. Once the control loop stabilizes, the sampled voltage at the FB pin equals the EA reference voltage of 2V. Based on this steady-state condition, the output voltage can be calculated as follows:

$$V_{FB} = (V_{OUT} + V_F + I_S R_S) \times \frac{N_A}{N_S} \times \frac{R_{FB1}}{R_{FB1} + R_{FB2}} = 2V$$

$$\text{Therefore } V_{OUT} = \frac{N_S}{N_A} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times 2V - (V_F + I_S R_S),$$

Output Voltage Sampling and Load Regulation Considerations: In the transformer, N_S and N_A represent the number of turns in the secondary output winding and the primary auxiliary winding, respectively. R_{FB1} and R_{FB2} are the voltage divider resistors used to sample the auxiliary winding voltage. V_F denotes the forward voltage drop of the output diode, I_S is the secondary output current, and R_S is the total resistance in the secondary output circuit. According to the voltage calculation formula, the term I_SxR_S affects the load regulation of the switching power supply. To minimize this effect, RVPW014 samples the voltage at the FB pin at the end of the transformer's demagnetization phase-when I_S is at its minimum. In Discontinuous Conduction Mode (DCM), when I_S=0, the output voltage is no longer affected by I_SxR_S, resulting in improved voltage accuracy. Therefore, to achieve high output voltage precision, it is recommended to design the power supply to operate in DCM. In Continuous Conduction Mode (CCM), the presence of I_SxR_S causes the output voltage to drop as the load increases.

Regardless of whether the converter operates in DCM or CCM, a sudden 20% drop in the FB voltage is used to detect the end of the demagnetization phase. At this moment, system latches the output voltage of the differential amplifier (EA). Since the EA output has a built-in delay, it does not immediately respond to rapid changes in FB voltage. Thus, latched voltage corresponds to the FB level just before the sudden drop, ensuring sampling accuracy. During the initial stage of demagnetization-immediately after the power MOSFET turns off-the resonance between the transformer's leakage inductance and parasitic capacitance can cause significant ringing in the FB voltage. To prevent incorrect sampling, a sampling delay $T_{D(SAMP)}$ is introduced, during this time the sampler remains inactive. When the sampler is active, during its sampling window T_{SAMP}, the peak-to-peak value of the resonant ripple on the FB pin should be limited to within 20% (approximately 400mV) of the steady-state FB voltage. When evaluating this at the auxiliary winding, the resistor divider ratio must be taken into account. To avoid distortion of the FB waveform, especially in high-frequency PSR (Primary Side Regulation) applications operating at several hundred kHz, it is strongly advised not to place filtering capacitors from FB to GND. Such capacitors can degrade waveform fidelity and impair output voltage accuracy. Additionally, under light-load conditions with short demagnetization times, even the parasitic capacitance of an oscilloscope probe can alter the FB waveform and cause output voltage deviations. Considering both the quality of the FB waveform and the power loss in the sampling resistors, it is recommended that R_{FB1} be selected within the range of 2.5kΩ to 6kΩ, with a typical value of 4kΩ.

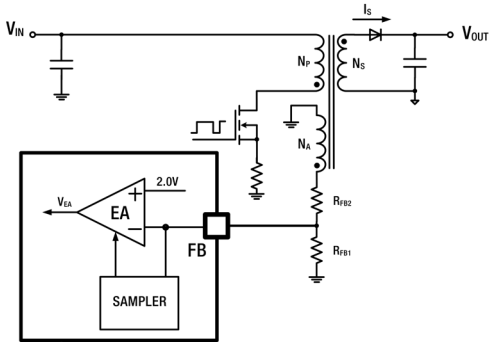


Fig. 21

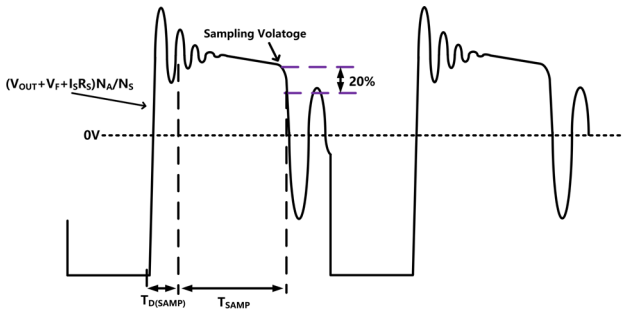


Fig. 22

Output Diode Temperature Compensation

RVPW014 includes a selectable temperature compensation feature, as illustrated in Figure 23. During the soft-start phase, the controller monitors the FB pin when the power MOSFET turns on. If no negative voltage is detected at the FB pin during this time, the temperature compensation enable switch remains open, disabling the temperature compensation function. Conversely, if a negative voltage is detected at FB during the MOSFET's turn-on phase, the enable switch closes, activating the temperature compensation circuit. When enabled, a positive temperature coefficient voltage V_{TC} is generated and buffered through a unity-gain amplifier. This voltage is then connected to the FB pin through a resistor R_{TC}=100kΩ. The voltage V_{TC} has a positive temperature coefficient of 3.5mV/°C, and at room temperature, V_{TC}= $V_{REF(REG)}$. This allows the RVPW014 to implement temperature compensation in primary-side regulation (PSR) flyback power supply applications. The degree of compensation is determined by the FB pin's voltage divider configuration, specifically the value of R_{FB2}. A calculation for determining R_{FB2} follows below.

$$V_{OUT} = \frac{N_S}{N_A} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times V_{REF(REG)} - \{\frac{N_S}{N_A} \times \frac{R_{FB2}}{R_{TC}} [V_{TC} - V_{REF(REG)}] + V_D\}$$

In the above equation, N_S and N_A represent the number of turns in the secondary and auxiliary windings of the transformer, respectively. V_D denotes the forward voltage drop across the output diode junction. To minimize the temperature coefficient of the output voltage, we set the derivative of the output voltage with respect to temperature to zero. This yields the condition for achieving temperature stability:

$$R_{FB2} = \frac{N_A}{N_S} \times \frac{\triangle V_D}{577.5mV} \times 100k\Omega$$

Let ΔV_D represent the change in the forward voltage drop of the output diode across the temperature range of -40°C to 125°C. To compensate for this temperature-induced variation in the output voltage, the appropriate value of R_{FB2} should be determined based on ΔV_D and this transformer turn the ratio N_S/N_A. Once R_{FB2} is established to achieve the desired temperature compensation, the value of R_{FB1} can then be calculated to set the target output voltage according to the required voltage division ratio

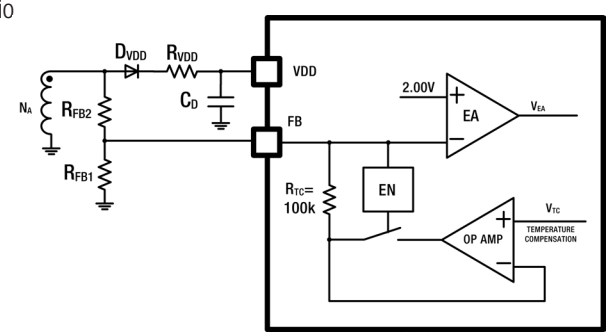


Fig. 23

OPERATION MODE

Feedback Port and Soft Start Up

As shown in Figure 24, when the chip is powered on or recovers from a protection condition, it enters a feedback mode selection stage during the first 12 switching cycles (from t_1 to t_2,) followed by a soft start phase (from t_2 to t_3). During the mode selection stage, the COM pin is pulled to approximately 3.2V, serving solely as a detection voltage for determining the type of feedback used. At this time, the internal PWM comparator threshold is intentionally limited to prevent high peak current in the power MOSFET. If an optocoupler is connected to the COM pin (indicating optocoupler feedback mode), the 3.2V detection voltage is maintained for the full 12-cycle duration. If the FB pin is used for primary-side regulation (PSR) feedback, and the controller detects this mode, the detection voltage lasts for only 2 switching cycles before exiting the mode selection stage. In optocoupler feedback mode, once the feedback mode has been determined, the internal soft-start voltage begins to rise gradually. This results in a controlled increase in duty cycle, ensuring a smooth startup without overshoot.

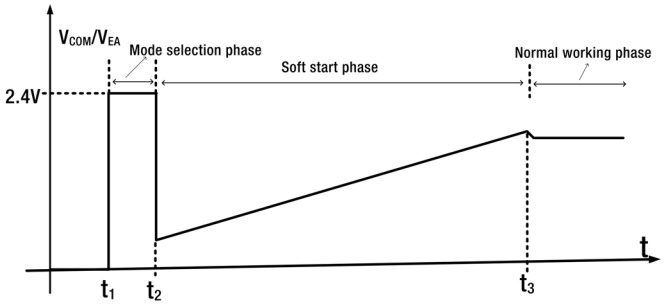


Fig. 24

Normal Operation State

Without triggering any protection logic, the output voltage of the converter is established during startup, forming a closed-loop feedback at time t_3 as shown in Figure 24. At this point, the soft-start phase ends, and the system transitions into the normal closed-loop regulation state. Depending on the output load conditions of the converter, the control voltage V_{COM} or V_{EA} rises to different levels by the end of soft start t_3 and stabilizes accordingly. The system may then operate either at the fixed oscillator frequency F_{OSC}, or in an analog frequency reduction mode (analog down-conversion), based on load demands and loop conditions.

Output Overload, SCP, OLP

Abnormal Operating Conditions and Protection Mechanism: Common abnormal conditions in converter operation include excessive output load beyond the design specification, output short circuits, poor soldering (e.g., virtual solder joints), or component failure. These issues can cause the feedback loop to enter an open-circuit state. RVPW014 incorporates a comprehensive protection mechanism to handle such scenarios, as illustrated in Figure 25. All three fault conditions may cause the duty cycle control voltage-either V_{COM} or V_{EA} to rise excessively, surpassing the open-loop protection threshold of 4.5V. If the V_{DD} voltage is below 5.3V, the protection threshold is adjusted to V_{DD}-0.8V. Once the fault occurs, the chip begins internal fault timing. If the abnormal condition has existed since the soft-start phase, timing starts from the first PWM pulse. If the overvoltage condition on the control voltage persists for more than 55ms (with the counter resetting if the condition is briefly interrupted), the controller enters a protection mode. This mode includes a shutdown interval of 730ms, after which the device will attempt to restart. In some cases, protection may be triggered earlier than 55ms. Specifically, overcurrent SCP protection is activated if the peak current through the power MOSFET exceeds 9.5A, while overvoltage protection is triggered if the VDD voltage exceeds 10V. These conditions also lead to immediate entry into protection mode. By observing the duration of the DRN output pulses and monitoring the VDD voltage prior to entering protection, the type of fault condition can be inferred. This helps in accurately diagnosing the cause of abnormal converter behavior and supports efficient fault analysis during system development or troubleshooting.

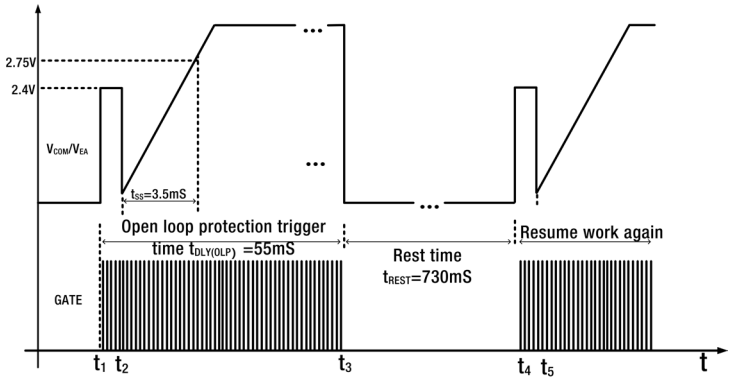


Fig. 25

APPLICATION CASES

Application Information

Startup Circuit

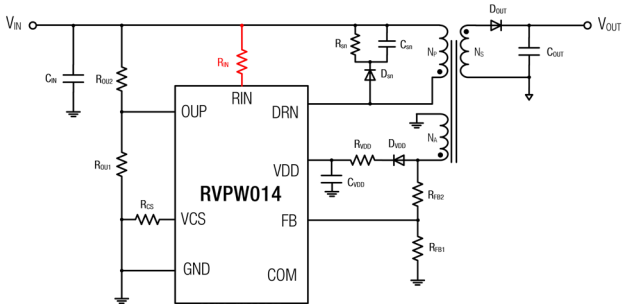


Fig. 26

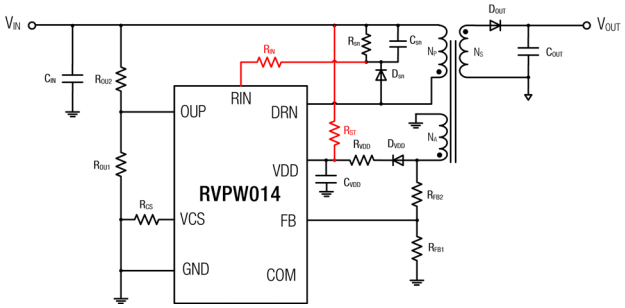


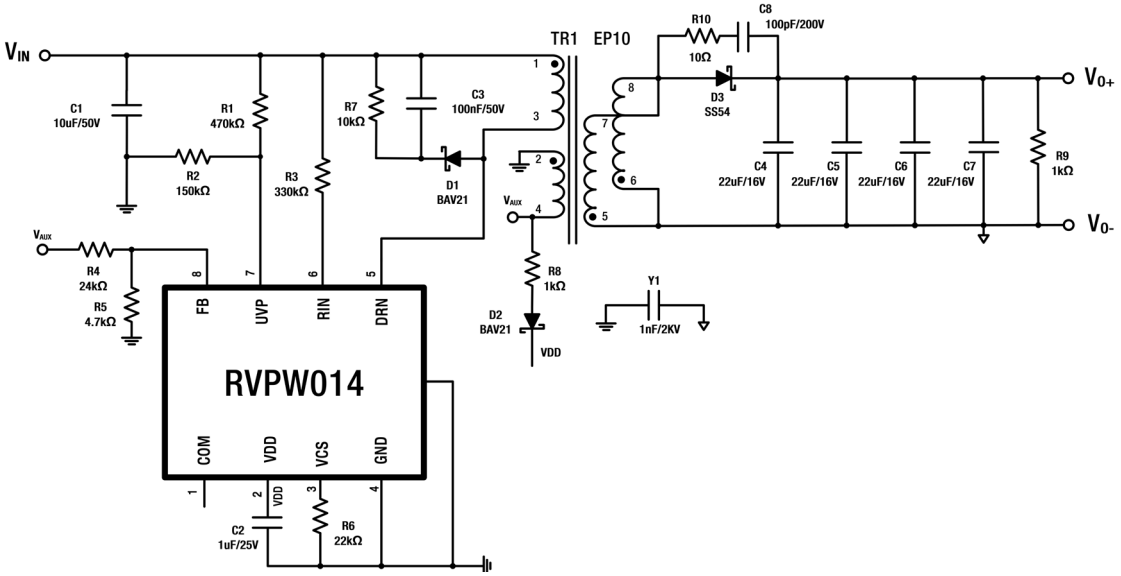
Fig. 27

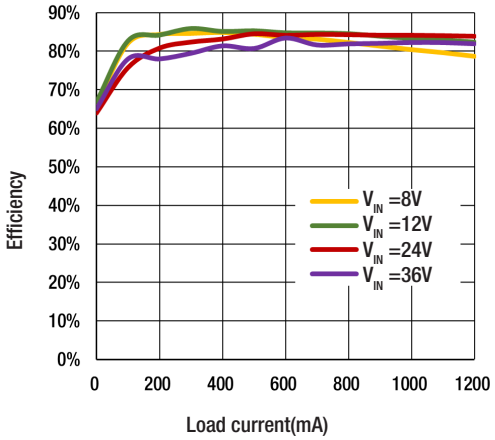
For applications where the minimum input voltage V_{IN} is greater than 6V, the startup circuit shown in Figure 26 should be used. In this configuration, resistor R_{IN} supplies bias current to the internal startup MOSFET, which in turn sources startup current from the DRN pin to the VDD pin. Once the converter's output voltage V_{OUT} is established, power is supplied to the chip via the auxiliary winding N_A. For applications where the minimum V_{IN} is less than 6V, the startup circuit shown in Figure 27 is recommended. In this case, R_{IN} should be connected to the RCD snubber (absorption) circuit, and an additional resistor R_{ST} must be connected between V_{IN} and VDD to ensure proper startup. The recommended value for R_{ST} is:

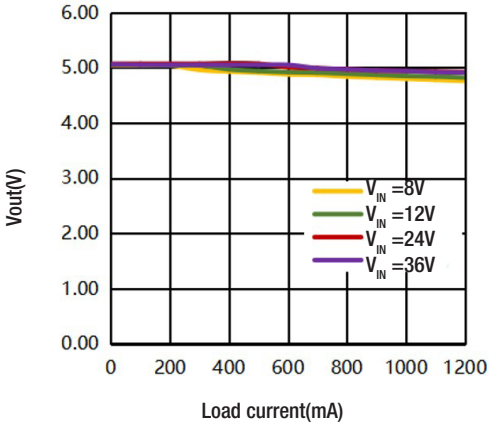
$$\frac{V_{IN(MAX)} - 9.5V}{4.5mA} < R_{ST} < \frac{V_{IN(MIN)} - 3.5V}{100\mu A}$$

Among them, $\mathbf{V_{IN(MIN)}}$ is the minimum input voltage, $V_{IN(MAX)}$ is the maximum input voltage, 3.5V is the upper limit of VDD startup voltage $V_{DD(ON)}$, 100uA is the upper limit of $I_{VDD(ON)}$, 9.5V is the lower limit of $V_{DD(OVP)}$, and 4.5mA is the lower limit of $I_{VDD(OVP)}$.

TYPICAL APPLICATIONS

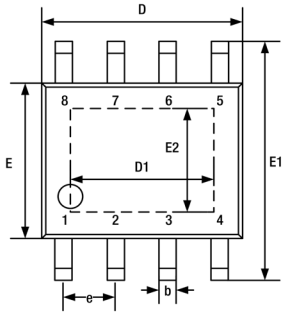




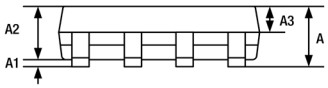


PACKAGING INFORMATION

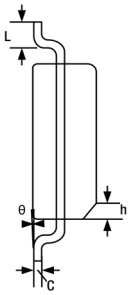
ESOP8



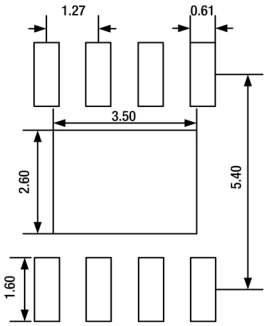
Package top view



Package front view



Package side view



Recommended solder pads

DIMENSIONTABLE			
SYMBOL	MILLIMETER		
	MINIMUM	NOMINAL	MAXIMUM
A	1.5	1.6	1.7
A1	0.04	---	0.12
A2	1.35	1.45	1.55
A3	0.65	0.7	0.75
b	0.35	---	0.5
c	0.19	---	0.25
D	4.8	4.9	5
D1	3.2	3.3	3.4
E	3.8	3.9	4
E1	5.8	6	6.2
E2	2.3	2.4	2.5
e	1.27 BSC		
h	0.3	---	0.5
L	0.5	---	0.8
θ	0°	---	8°

ORDER INFORMATION

Device	Package Type	PIN	Packaging Method	QTY	Marking Code*	MSL
RVPW014-FJ1-R	ESOP8	8	Tape and Reel	4000	RVPW014	MSL-3

*Marking Code :
RVPW014—— Product Code