RVPW011 Current Mode PWM Controller

5-50VIN/90V/40mΩ Power MOSFET

FEATURES

- 5V~50V Ultra-wide Range of Input Voltage
- Suitable for Primary Side Feedback Flyback Converter
- Minimum Sampling Time as Low as 0.4uS
- Boundary Conduction Mode at the Heavy Load
- Decrease the Operating Frequency to Improve Efficiency Under Light-load Conditions
- Integrated 90V/40mΩ LDMOS
- Integrated Lossless Current Sampling
- Programmable Peak Current
- Programmable Power MOSFET Driving Speed
- Programmable Feedforward Compensation
- Programmable Soft Start
- Programmable Input Undervoltage and Overvoltage Protection
- Short Circuit Protection, and Over Temperature Protection
- Internal Loop Compensation
- Current Less Than 0.1μA When Enable Turn Off
- Output Diode Voltage Drop Temperature Compensation
- QFN5x5 Strong Heat Dissipation Packaging

APPLICATIONS

- Energy Storage Isolation Power Converters
- Industrial Power Conversion
- BMS Auxiliary Power Supplies
- POE Power Supplies
- Isolation Communication Power Supplies

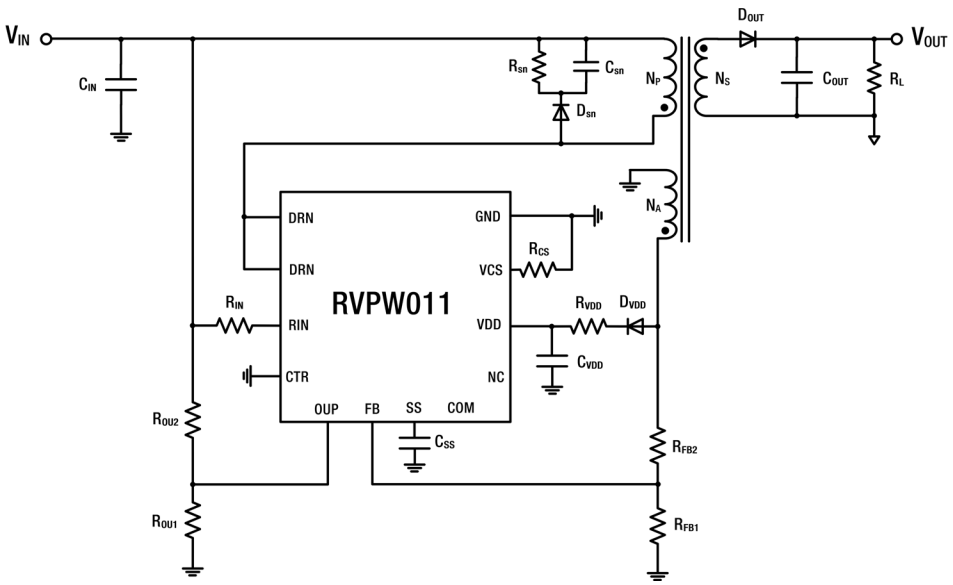
DESCRIPTION

RVPW011 is a flyback converter that achieves voltage regulation by sampling the primary winding of the transformer, supporting primary-side regulation (PSR) feedback at operating frequencies in the hundreds of kHz. Its internal output voltage sampling circuit operates with a sampling voltage pulse as narrow as 400ns. Equipped with an internal loop compensation circuit and fast dynamic response capability, the RVPW011 ensures excellent system stability and dynamic performance for switching power supplies. Designed for low-voltage operation, the RVPW011 supports input voltages as low as 5V. It features a low on-resistance internal MOSFET of just 40mΩ. Combined with its thermally efficient 5mm×5mm QFN package, the device can deliver output power up to 30W. RVPW011 integrates multiple control functions with minimal external components, allowing designers to tailor the system to specific application needs. It enables startup, feedforward compensation, and control over the shutdown speed of the internal power MOSFET via external resistors. The peak current of the power MOSFET can also be programmed using a resistor, enabling “lossless” current sensing. Input undervoltage and overvoltage protection thresholds can be set simultaneously using two resistors. Additionally, the soft-start time is programmable through an external capacitor, allowing for optimized performance based on the application. To ensure robust and reliable operation, the RVPW011 incorporates built-in protections including overload protection, output short-circuit protection, output overvoltage protection, and over-temperature protection. These protection mechanisms support automatic recovery after fault conditions are resolved, maximizing the reliability and resilience of the overall power supply system.

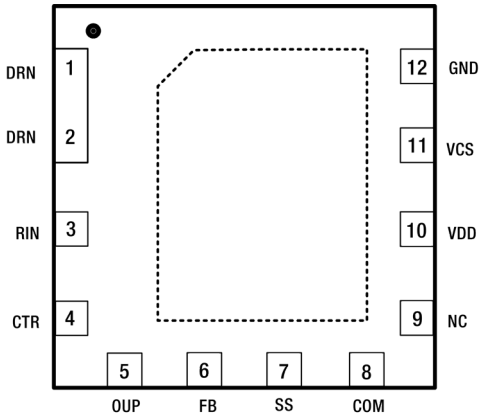
Device Information

Part Number	Package	Weight(mg)	Size	SPQ
RVPW011	QFN5x5	61.12	5.0 mm x 5.0 mm	4000

SIMPLIFIED SCHEMATIC



PINOUT AND FUNCTIONS



NAME	QFN12 PIN NUMBER	TYPE	DESCRIPTION
DRN	1,2	O	Pins 1 and 2 are connected together, they are the drain of the internal LDMOS.
RIN	3	I	Connecting an external resistor to V_{IN} can achieve the functions of starting,power MOSFET shutdown speed rate adjustment, and feedforward compensation.
CTR	4	I	Control pin. When CTR is high level and the OUP voltage is greater than the threshold voltage for turning on the RIN function, the DRN pin stops the driving signal and COM pin is pulled up to a high level. This function is designed for the control logic of bidirectional isolation converter, if this function is not needed, connect CTR to GND.
OUP	5	I	Input overvoltage/undervoltage protection multiplexed pin. The input undervoltage protection threshold and recovery threshold can be designed by the proportional coefficient of the peripheral voltage divider resistors, and the input overvoltage protection threshold can be designed by the resistance value of the voltage divider resistors. If OUP is lower than the threshold voltage of 0.75V for activating the RIN function, the internal start-up circuit is turned off and the switching converter is in the ultra-low-power standby mode.
FB	6	I	Output voltage feedback pin. This port can sample the output voltage of the switching power supply through auxiliary winding or directly using two voltage divider resistors.The sampled voltage is modulated by an error amplifier to adjust the duty cycle of the power MOSFET, in order to stabilize the output voltage of the switching power supply.
SS	7	I	Soft-start pin. The internal 27μA current source flows out of this pin to charge the external soft-start capacitor, and the ramp voltage generated by charging controls the error amplifier output voltage VEA rising gradually , which controls the duty cycle of the converter unfolding gradually when the converter start-up.
COM	8	I	Enable optocoupler driving pin of bidirectional isolated converter.
NC	9	-	No function pin, no electrical connection.
VDD	10	P	The power supply port of the chip, V_{DD} generates an internal power supply VCC through a low dropout voltage LDO to supply power to the control circuit, the LDO operates in the linear region with a V_{CC} voltage of 5.3V, and operates in the dropout voltage region, there is a dropout voltage approximately 0.3V between V_{DD} and $V_{CC.}$ V_{DD} also has a voltage clamp function, the clamping voltage is about 10V, if the current absorbed by the clamp exceeds 6.3mA, the power MOSFET is prohibited from being turned on and enters a self-recovery protection state.
VCS	11	I	Peak current threshold setting pin. Connect a resistor of tens of KΩ to GND, and set the maximum and minimum peak current range for internal lossless current sampling.
GND	12	P	The reference ground of the chip. This port is the signal ground for internal control logic and also the source of the internal LDMOS.
EP	-	P	Die bonding pad. This pad is bonded to the bottom of die. and can be connected to GND. The pad must be fully connected to the PCB board to facilitate heat of die dissipation .

SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
RIN, OUP, CTR to GND	VRIN,VOUP,VCTR	-0.3	35	V
VDD to GND	VDD	-0.3	13	
DRN to GND	V_{DRN}	-1.3	95	
DRN to GND (transient<20nS)		-2.5		
FB to GND	V_{FB}	-0.5	6	
The peak current of FB to GND	$I_{FB\ (PEAK)}$		-2.5	mA
Other pins to GND	V_{COM}, V_{CS}	-0.3	6	V
Maximum operating junction temperature	V_{JMAX}		150	°C

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body mode HBM, per ESDA/JEDEC JS-001-2023, (Zap 1 pulse, Interval:>=0.1S)	±2000	V
		Charged Device Model CDM, per ESDA/JEDEC JS-002-2022	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM can be safely manufactured under standard ESD control processes.
(2) JEDEC document JEP157 states that 250-V CDM can be safely manufactured under standard ESD control processes.

Thermal Resistance

Packaging	θ_{JA}	Ψ_{JT}	UNIT
QFN5x5	62.5	3.11	°C/W

Note: Measured on a test board with 1oz copper (7.62cm × 11.43cm).

Recommended Operatings Conditions

		MIN	TYP	MAX	UNIT
Power MOSFET drain voltage	V_{DRN}			85	V
OUP pin voltage	V_{OUP}			15	
VDD input voltage	V_{DD}	2.5		10	
VCS external resistor	R_{CS}	10			kΩ
RIN external resistor	R_{IN}			1	MΩ
FB Current	I_{FB}	-2			mA
Ambient temperature	T_A	-40		125	°C

Electrical Characteristics

Unless otherwise specified, the following parameters were measured under the condition of V_{DD}= 7V and temperature T=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
$V_{DD(ON)}$	VDD turn on threshold	V_{DD} rising	2.1	2.3	2.5	V
$V_{DD(OFF)}$	VDD turn off threshold	V_{DD} falling	2.0	2.2	2.4	V
$I_{VDD(ON)}$	VDD turn on current	V_{DD} rising		54	100	uA
$I_{VDD(OP)}$	Quiescent current at startup frequency	f_{DRN}=67kHz	1.5	2.2	2.8	mA
$I_{VDD(UVP)}$	Operating current under input voltage	OUP= 1.5V		220	300	uA
$V_{DD(DMAX)}$	MOSFET for starting up supply voltage@D_{MAX}	VCS float	4	4.8	5.5	V
$V_{BV(DIODE)}$	Break voltage of anti reflow diode		37			V
$V_{DD(OVP)}$	VDD overvoltage shutdown threshold	V_{DD} rising	9.5	10	10.8	V
$I_{VDD(OVP)}$	VDD absorbs current during overvoltage protection	V_{DD}= $V_{DD(OVP)}$	5.5	6.3	7.5	mA
RIN						
V_{ZB}	MOSFET for starting up bias Voltage	I_{RIN}=1uA	6.0	6.9	8.0	V
$I_{RIN(OFF)}$	Enable shutdown current	OUP=0V		0.1	1	uA
$R_{IN(IN)}$	Input resistance			100		kΩ
VCS						
$V_{CS(MAX)}$	Maximum threshold voltage		1.85	2.0	2.15	V
$V_{CS(MIN)}$	Minimum threshold voltage		200	300	380	mV
k_{CS}	Proportional coefficient between peak current of power MOSFET and VCS current		40000	50000	60000	A/A
OUP						
$V_{OUP(ON)}$	Undervoltage protection turn-on voltage		1.9	2.0	2.1	V
$V_{OUP(OFF)}$	Undervoltage protection turn-off voltage		1.67	1.75	1.83	V
$V_{OUP(RINON)}$	Threshold voltage for enable the RIN function		0.55	0.75	1.1	V
$V_{OUP(OC)}$	Input overcurrent protection clamp voltage	I_{OUP}=50uA injected into OUP pin	2.1	2.2	2.4	V
$I_{OUP(OFF)}$	Input overcurrent protection comparison current	I_{OUP} gradually increasing	92	100	108	uA
$I_{OUP(ON)}$	Input overcurrent protection recovery comparison current	I_{OUP} gradually decreasing	83	90	97	uA
FB						
$V_{REF(REG)}$	Reference voltage of EA		1.97	2.0	2.03	V
A_V	Low frequency gain of EA			1400		V/V
$T_{D(SAMP)}$	Delay time of sampling			252	350	nS
K_{VTC}	The temperature coefficient of temperature compensation voltage			3.5		mV/°C
I_{FB}	Pin output current			-40		nA
COM						
V_{COMH}	Open loop voltage		5.0	5.3	5.3	V
I_{COM}	Short-circuit current	V_{COM}= 0V, V_{DD}=7V, CTR=3V	1.06	1.38	1.65	mA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CTR						
$V_{CTR(ON)}$	V_{CTR} turn on threshold	V_{OUP}>1.1V, V_{CTR} gradually rising	1.35	1.87	2.4	V
$V_{HYS(OFF)}$	Hysteresis voltage	V_{OUP}>1.1V, V_{CTR} gradually falling		0.14		V
R_{CTR}	Pull-down resistance		280	400	520	kΩ
SS						
$V_{SS(OPEN)}$	open-circuit voltage of soft-start pin		5.0	5.3	5.6	V
I_{SS}	External soft start current		22	27	33	uA
$R_{SS(DIS)}$	Bleeder resistor			173		Ω
DRN						
$R_{DS(ON)}$	MOSFET on-state resistance	I_{DS}= 4A, T=25°C		40		mΩ
		I_{DS}= 4A, T=125°C		63		mΩ
f_{ST}	Start-up frequency	FB=0	60	67	74	kHz
f_{OSC}	Maximum operating frequency		300	330	360	kHz
f_{MIN}	Minimum operating frequency		6	9	12	kHz
$t_{ON(MIN)}$	Minimum conduction time	VCS float, drain connected to a 120Ω pull-up resistor and pull-up voltage 24V		250		nS
Other Protection Functions						
T_{SHDN}	Over temperature protection threshold		150	168	178	°C
$T_{SHDN(HYS)}$	Over temperature protection hysteresis			18		°C
$t_{DLY(OLP)}$	OLP trigger time	From V_{COM}>$V_{COM(OLP)}$ to enter protection		66		mS
t_{REST}	Rest time after self recovery protection			2		S

Typical Characteristics

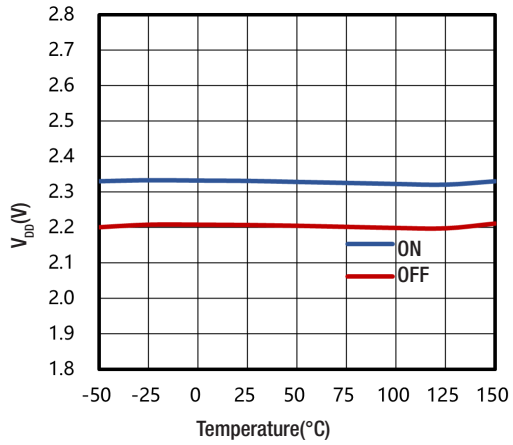


Fig. 1 $V_{DD(ON)}$ and $V_{DD(OFF)}$ vs Temperature

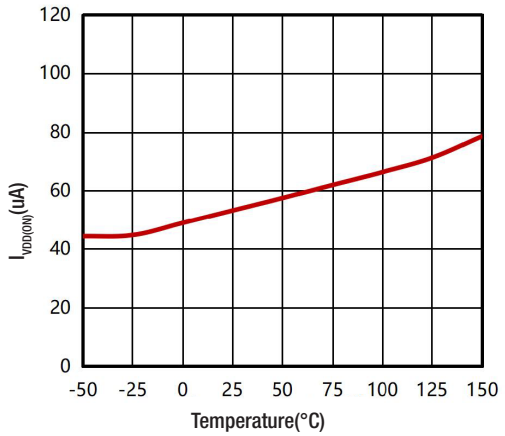


Fig 2 $I_{VDD(ON)}$ vs Temperature

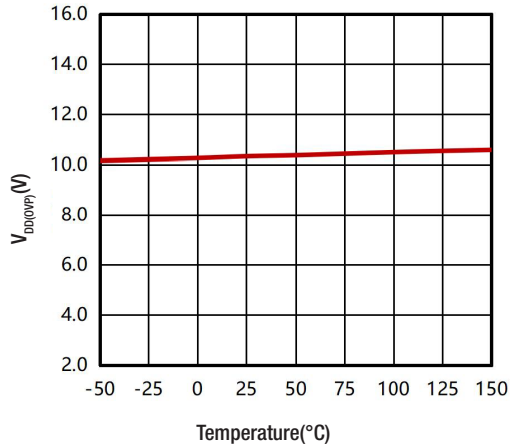


Fig. 3 $V_{DD(OVP)}$ vs Temperature

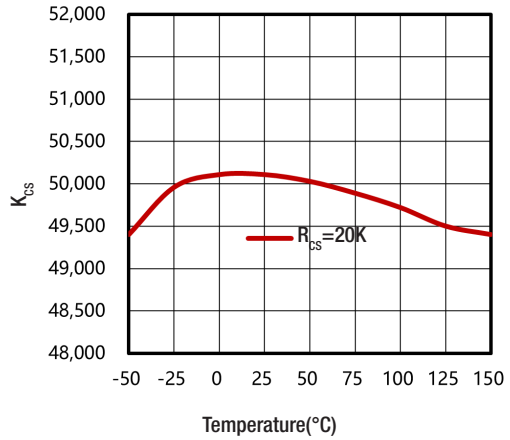


Fig. 4 K_{CS} vs Temperature

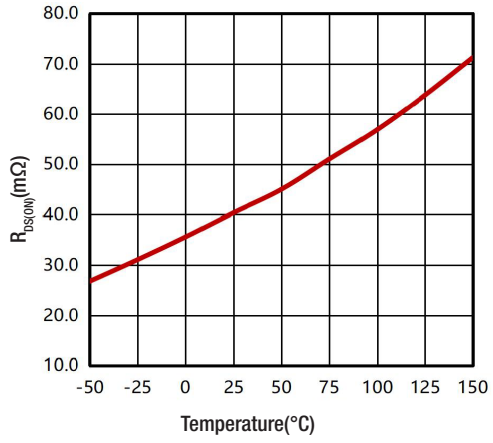


Fig. 5 $R_{DS(ON)}$ vs Temperature

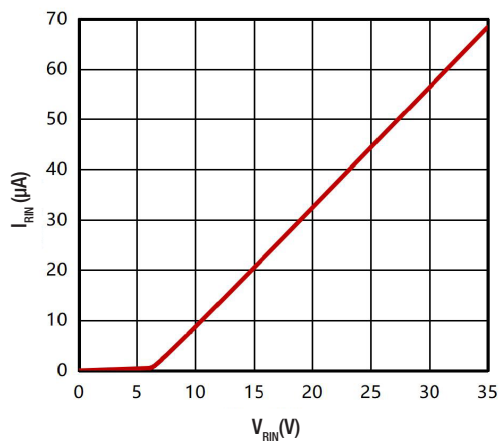


Fig. 6 I_{RIN} vs V_{RIN}

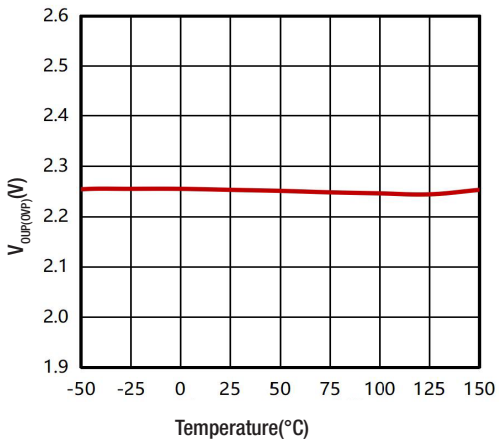


Fig. 7 $V_{OUP(OC)}$ vs Temperature

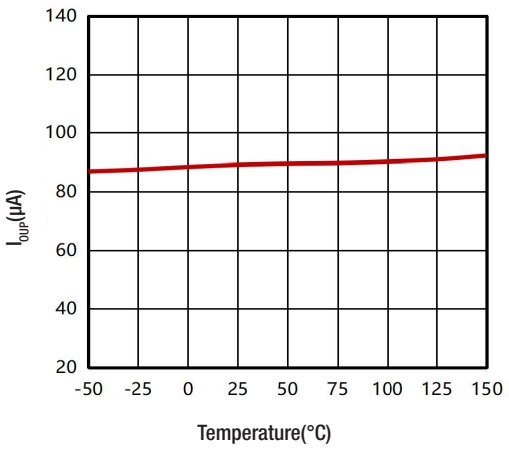


Fig. 8 $I_{OUP(ON)}$ vs Temperature

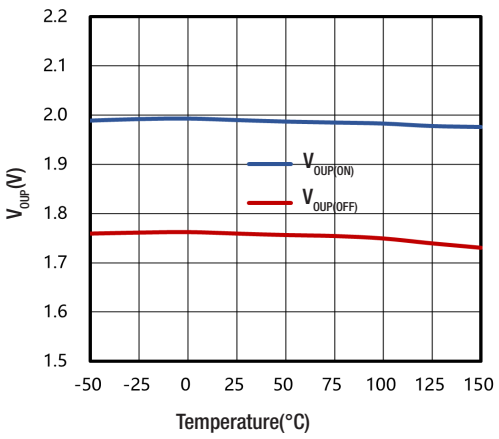


Fig. 9 $V_{OUP(ON)}$ and $V_{0kUP(OFF)}$ vs Temperature

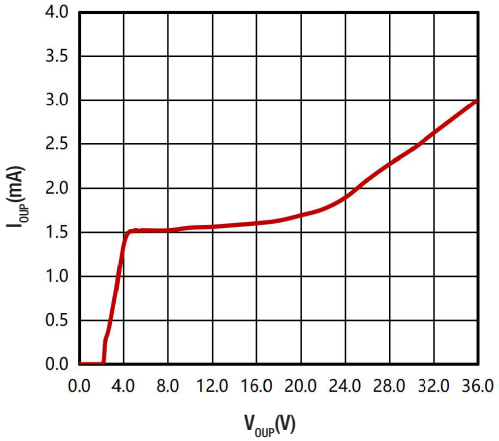


Fig. 10 I_{OUP} vs V_{OUP}

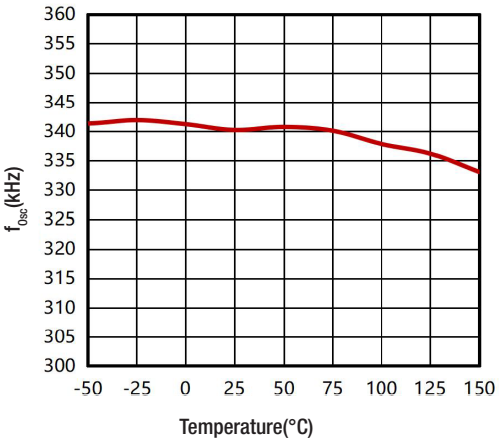


Fig. 11 f_{OSC} vs Temperature

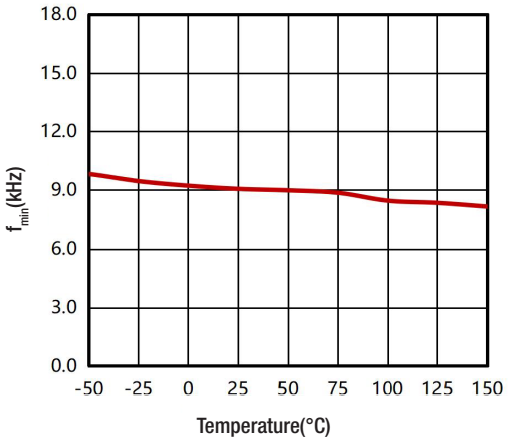


Fig. 12 f_{MIN} vs Temperature

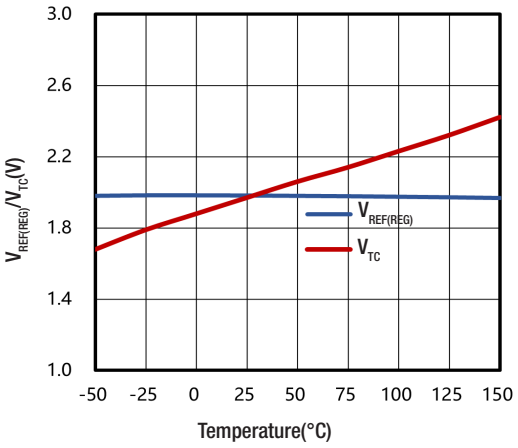


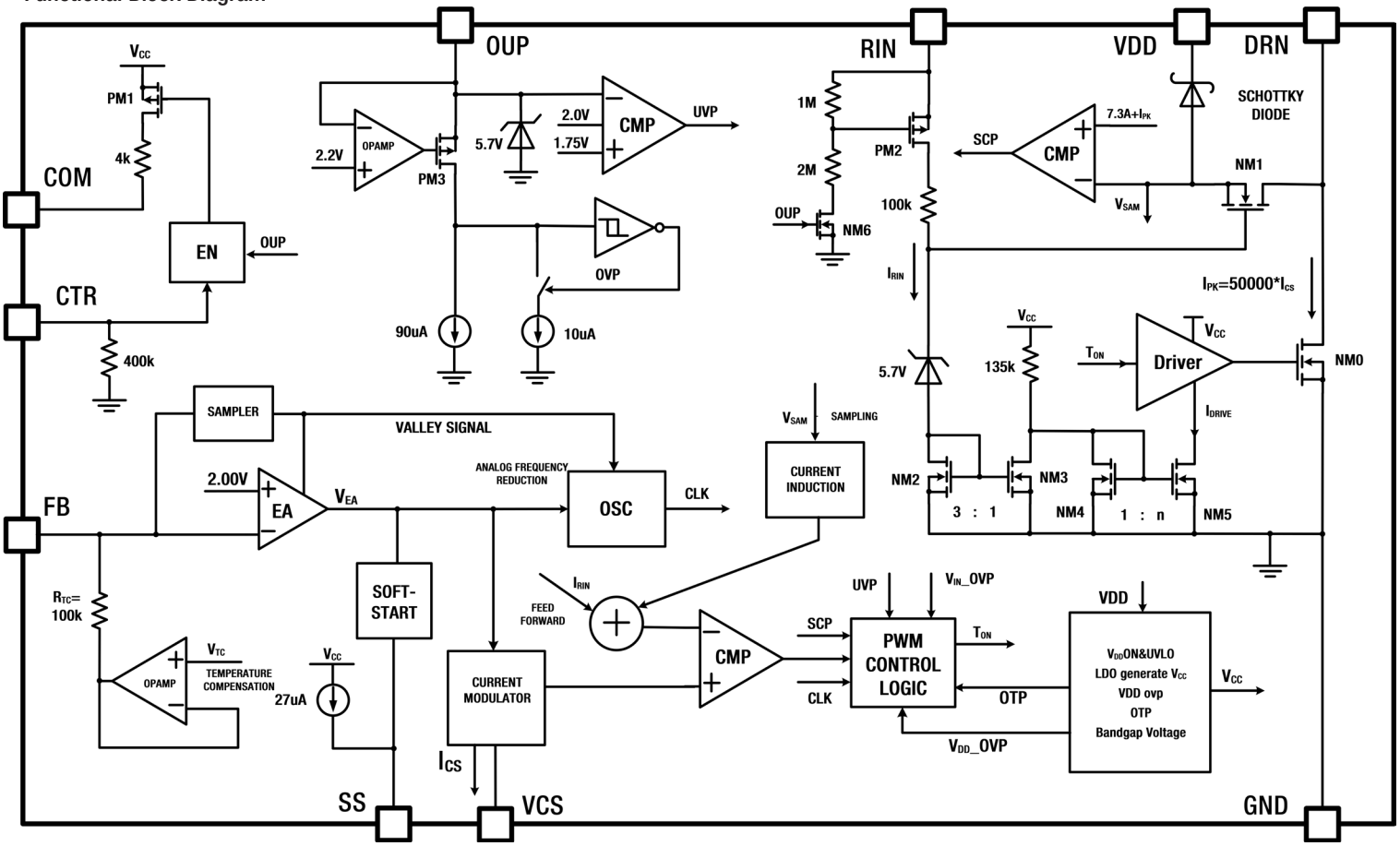
Fig. 13 $V_{REF(REG)}$ and V_{TC} vs Temperature

DETAILED DESCRIPTION

Overview

RVPW011 is a current-mode PWM converter that integrates control circuitry and a power MOSFET onto a single chip using advanced BCD technology, making it well-suited for flyback power converter applications. By sampling the output voltage through the transformer windings, the device eliminates the need for isolation components such as optocouplers and external feedback devices like the TL431. This results in a simplified peripheral circuit and reduced system cost. During heavy load conditions, the converter turns on at the first resonant valley following transformer degaussing, operating in boundary conduction mode (BCM). This mode of operation delivers high conversion efficiency and excellent electromagnetic interference (EMI) performance. The RVPW011 integrates a power nLDMOS with low internal resistance, enabling output power up to 30W. The peak current limit of the internal power MOSFET is programmable, allowing precise implementation of BCM timing under typical load conditions. Beyond peak current programming, the RVPW011 offers extensive configurability to suit various application needs. Designers can adjust the power MOSFET shutdown speed, implement feedforward compensation, program the soft-start time, and apply temperature compensation for the output diode. Additionally, both input undervoltage and overvoltage protection thresholds can be configured externally. Designed to support miniaturization, the RVPW011 is ideal for switching power supplies that require a wide input voltage range. It is widely used in applications such as IGBT-based motor drives, industrial automation systems, medical instruments, and other high-performance environments.

Functional Block Diagram



Feature Description

Function and Resistance Value of External Resistor R_{IN}

As illustrated in Figure 14, a resistor R_{IN} is connected between the RIN pin of the RVPW011 and the converter's input voltage (V_{IN}). This resistor serves three key functions: 1. Startup Biasing: It provides the necessary bias current to initiate the startup of the internal MOSFET (NM1). 2. Power MOSFET Turn-Off Control: It programs the turn-off speed of the internal power MOSFET (NM0). 3. Feedforward Compensation: It supports the implementation of feedforward compensation for improved dynamic performance. The enable/disable behavior of the RIN function is controlled by the voltage at the OUP pin. When OUP is connected to ground (GND), PM2 remains in the cut-off state, effectively disabling the RIN function and achieving zero standby power consumption. The RIN function is enabled only when the OUP voltage exceeds the NM6 turn-on threshold (approximately 1V), allowing PM2 to conduct.

Startup and Power Supply: When the RIN function is enabled, it delivers bias current through a 5.7V Zener diode and NM2, which is connected between the gate and source of NM1. The total voltage provided-comprising the Zener breakdown voltage and the gate-source voltage of NM2-is approximately 6.9V, which is sufficient to bias NM1 and initiate startup. This startup current charges the VDD capacitor via the drain pin (DRN) of the power MOSFET NM0, passing through NM1 and a Schottky diode. Once the converter's output voltage is properly established, it is recommended to power the VDD pin using an auxiliary transformer winding. This is due to the significant power loss associated with the internal startup circuitry. To ensure that the internal startup circuit is fully deactivated, the VDD voltage should exceed 6V during operation. VDD pin also includes voltage clamping and overvoltage protection features. The clamp voltage is set to 10V. If the current absorbed by the clamp exceeds 6.3mA, the overvoltage protection mechanism is triggered, placing the chip into a protection mode. In flyback converter applications, this behavior can be leveraged for output overvoltage protection, by utilizing the proportional relationship between the auxiliary and secondary winding voltages of the transformer.

Switching speed of power MOSFET NM0: The input current I_{RIN} of the pin RIN is calculated to generate the driving current I_{DRIVE}, and their relationship is:

$$\frac{I_{DRIVE}}{n} = \frac{V_{CC} - V_{GS4}}{135K\Omega} - \frac{1}{3} \times \frac{V_{IN} - 5.7V - V_{GS2}}{R_{IN} + 100K\Omega}$$

In the equation described earlier, the internal supply voltage V_{CC} is 5.3V, and the gate-source voltages V_{GS2} and V_{GS4} are approximately 1.2V. If an external resistor R_{IN} is set to 330kΩ and the equation yields a result of zero, this corresponds to a condition where I_{DRIVE}=0. At this point, when the input voltage V_{IN} reaches 46V, the gate drive circuit switches the power MOSFET (NM0) on and off using only its intrinsic driving capability. Under these conditions, the turn-off speed of NM0 is at its slowest. When I_{DRIVE}>0, the turn-off speed of NM0 increases accordingly. From this relationship, two key observations can be made. First, the shutdown speed of NM0 can be programmed by adjusting the value of R_{IN}. A larger resistance results in a smaller I_{DRIVE}, which in turn speeds up the shutdown of NM0. Second, as the input voltage increases, I_{DRIVE} decreases, which slows down the turn-off of NM0. This reduction in switching speed at high input voltages helps suppress voltage spikes caused by transformer leakage inductance, improving system reliability under high-line conditions.

Feedforward compensation function; is realized by proportionally mirroring the current I_{RIN} through NM2 and using it as a feedforward compensation current. This mirrored current is superimposed with both the sampling current from the power MOSFET NM0 and the slope compensation current, and together they serve as the input to the PWM comparator. As input voltage increases, the feedforward compensation current also increases, which helps minimize variations in overcurrent thresholds between low and high input voltages. This compensates for delay in PWM comparison and gate drive, improving overall control accuracy.

R_{IN} resistor design; the chip internally includes a 100kΩ resistor in series with the external R_{IN} pin. This serves two purposes. First, it drops part of the voltage across an internal element, ensuring that even ultra-small package resistors with limited creepage distance can operate safely. Second, in low-voltage applications, the external R_{IN} resistor may be omitted entirely, with the internal resistor alone providing sufficient bias for NM1 startup. Since there is no strict requirement for the R_{IN} value for startup purposes, its selection primarily balances the trade-off between NM0 shutdown speed and feedforward compensation performance. In practical applications, R_{IN} is typically selected within the range of several hundred kΩ to 1MΩ.

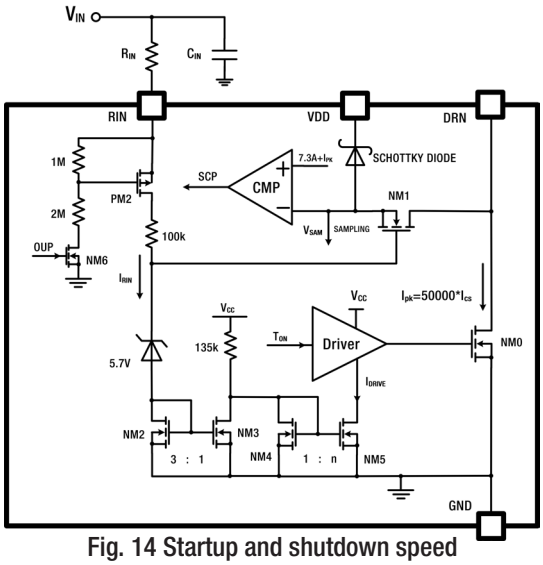


Fig. 14 Startup and shutdown speed

Short Circuit Protection

RVPW011 includes an integrated output short-circuit protection feature, which is implemented through two complementary mechanisms to ensure system safety and reliability. The first mechanism is based on current sensing. During an output short-circuit condition, the current flowing through the internal power MOSFET (NM0) rapidly increases. When this current reaches a predefined threshold, the overcurrent protection (OCP) is triggered. At that moment, the DRN pin immediately stops outputting switching pulses, and the device enters a protection mode. After a fixed rest period, denoted as t_{REST}, the converter attempts to restart operation.

As illustrated in Figure 14, the overcurrent threshold is defined as 7.3A+I_{PK}, where I_{PK} is the maximum peak current under short-circuit conditions. This peak current is determined by the value of the external current sense resistor (VCS).

The second protection mechanism monitors the FB (feedback) pin voltage. In a short-circuit condition, the output voltage collapses, causing the FB voltage to remain very low. As a result, the controller is unable to detect the transformer's voltage valley, which is essential for timing in boundary conduction mode. When this occurs, an internal counter begins timing. If the valley detection failure persists for a duration longer than the delay time $t_{DLY(OLP)}$, the device enters an open-loop protection state. In this state, DRN pulse output is disabled, and the converter stops switching. After the rest period t_{REST}, the controller attempts to resume normal operation. These two protection modes ensure both immediate response to overcurrent events and fail-safe behavior during sustained fault conditions, enhancing the robustness of the RVPW011 in demanding applications.

Enable Control Logic

RVPW011 is designed with two distinct turn-off states to accommodate various power system control requirements. In the first state, when the voltage at the OUP pin falls below the threshold $V_{OUP(RINON)}$, the internal startup circuit is completely disabled. As a result, the VDD voltage drops to zero, placing the device into a full shutdown mode with zero quiescent power consumption. In the second state, the voltage at the OUP pin exceeds $V_{OUP(RINON)}$, activating the internal startup circuit. VDD rises into its normal operating range. However, if the CTR pin voltage remains higher than its turn-on threshold, the internal driver circuit actively pulls the gate of the power MOSFET (NM0) low, preventing any output from the DRN pin. Meanwhile, the COM pin provides a pull-up drive current. This dual-control logic is specifically designed to support bidirectional isolated converter architectures. In such configurations, when both OUP and CTR are at high levels simultaneously, the RVPW011 disables its internal power MOSFET (NM0), halting its primary-side switching. At the same time, the COM pin drives an optocoupler, which signals the secondary-side PWM controller of the bidirectional converter to begin operation-enabling reverse power transmission. This flexible control mechanism makes the RVPW011 ideal for systems that require coordinated handoff between primary and secondary controllers in bidirectional or energy-recovery applications.

Input Over/Under Voltage Protection

As shown in Figure 15, the input overvoltage protection (OVP) and undervoltage protection (UVP) functions of the RVPW011 are implemented through a single pin, OUP, with both protection thresholds programmable to suit specific application requirements. The operating principle is as follows: when the voltage at the OUP pin is below 2.2V, the pin draws no current. Under this condition, the turn-on and turn-off thresholds for VIN undervoltage protection can be accurately calculated using external resistor divider values, providing a simple and flexible method for setting the input voltage protection levels.

$$V_{INON(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU2}} \times 2V$$

$$V_{INOFF(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU2}} \times 1.75V$$

When the voltage at the OUP pin exceeds 2.2V, the pin begins to draw current and stabilizes at this voltage level. If the current drawn by the pin exceeds 100μA, it is recognized as an input overcurrent condition at the OUP pin, indicating that the input voltage has surpassed the overvoltage protection threshold. In this case, the RVPW011 stops switching the internal power MOSFET (NM0) and enters a protection state. As the input voltage decreases and the drawn current falls below 90μA, the device exits the protection state and resumes normal operation. The input overvoltage protection threshold and its corresponding recovery voltage can be calculated based on the resistor divider network as follows:

$$V_{INOFF(OVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2.2V + 100\mu A \times R_{OU2}$$

$$V_{INON(OVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2.2V + 90\mu A \times R_{OU2}$$

When designing the resistance values of R_{OU1} and R_{OU2} , a more practical formula can be obtained to quickly determine the resistance:

$$R_{OU2} = \frac{V_{INOFF(OVP)} - 1.1 \times V_{INON(UVP)}}{100\mu A}$$

As long as the operating range of the input voltage of the converter is determined, R_{OU2} can be calculated,and then combined with the undervoltage protection formula, R_{OU1} can be calculated.

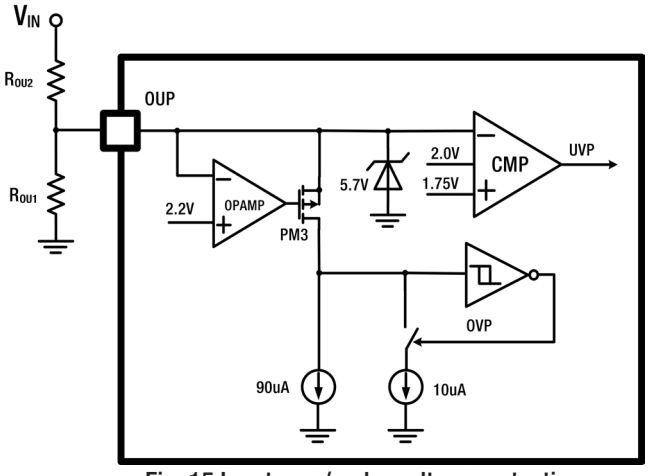


Fig. 15 Input over/under voltage protection

PWM and PFM Control

Current Sampling:The conduction voltage drop across the power MOSFET NM0 is sensed at its source to initiate the operation of NM1. This voltage is then replicated using an operational amplifier and applied to a sampling MOSFET, which is of the same type as NM0 but has a higher internal resistance. As a result, a current proportional to the peak current I_{PK} of NM0 is induced in the sampling MOSFET.

Current Modulator: The pulse width modulation voltage V_{EA} generates a corresponding modulation current through the external resistor connected to the V_{CS} pin, as illustrated in Figure 16. The relationship between V_{EA}, V_{CS}, and the switching frequency f_{DRN} determines the behavior of the current modulator. As V_{EA} varies, V_{CS} follows accordingly, producing a modulation current through the external resistor to regulate the peak current of the power MOSFET NM0 and adjust the converter's output voltage. When V_{EA} exceeds 2.75V, V_{CS} reaches its maximum value, $V_{CS(MAX)}$, thereby limiting the peak current of NM0. To allow sufficient demagnetization time for accurate output voltage sampling at the FB pin, the minimum value of V_{CS} is clamped at $V_{CS(MIN)}$=300mV. This ensures a minimum energy transfer from the transformer and requires additional dummy loads to prevent the output voltage from rising excessively under no-load conditions.

PWM Control: The pulse width modulation PWM current serves as the positive input to the PWM comparator, while the sum of the induced current, slope compensation current, and feedforward compensation current forms the negative input. The comparator outputs the pulse width signal that drives NM0, regulating the converter's output voltage and maintaining it at the rated value. In the BCM operating state, the output power and frequency can be calculated by the formula:

$$P_{OUT} = 0.5 \times I_{PK} \times V_{IN} \times D \times \eta$$

Where I_{PK} is the peak current of the power MOSFET, V_{IN} is the input voltage, η is the conversion efficiency of the transformer, and D is the duty cycle, which is:

$$D = \frac{N_{PS} \times (V_{OUT} + V_F)}{N_{PS} \times (V_{OUT} + V_F) + V_{IN}}$$

where N_{PS} is the transformer primary and secondary winding turns ratio, V_F is the output diode voltage drop.The formula for the operating frequency is as follows:

$$f_{DRN} = \frac{V_{IN}}{L_P \times I_{PK}} \times \frac{N_{PS} \times (V_{OUT} + V_F)}{N_{PS} \times (V_{OUT} + V_F) + V_{IN}}$$

PFM Control: RVPW011 supports Pulse Frequency Modulation (PFM) control and operates in three distinct modes depending on the load conditions, each with a different frequency variation pattern. First, in the Boundary Conduction Mode (BCM)-as shown in stage C to D of Figure 16-the operating frequency increases as the converter load decreases. This occurs because the modulation voltage V_{EA} gradually drops, leading to a reduction in the peak current. Consequently, both the excitation and demagnetization times of the transformer decrease, resulting in a higher switching frequency. This frequency behavior aligns with the f_{DRN} formula and is characteristic of normal BCM operation. Second, as the load continues to decrease, particularly under light-load and high input voltage conditions, the switching frequency may attempt to exceed the maximum frequency limit of 330kHz. When this limit is reached, the converter transitions out of BCM and into Discontinuous Conduction Mode (DCM). In this state, switching no longer occurs at the first resonant valley. This transition is illustrated by the red solid line in the B to C stages of Figure 16, indicating a fixed maximum frequency operation. Third, under even lighter load conditions, the RVPW011 activates its analog frequency reduction feature to enhance light-load efficiency and minimize no-load power consumption. As the converter load continues to decrease, V_{EA} drops further, leading to a controlled reduction in switching frequency. However, due to the nature of primary-side regulation (PSR), output voltage sampling can only occur during the transformer's demagnetization phase. To ensure stable operation and accurate voltage regulation, the switching frequency is limited to a minimum of 9kHz(FMIN). This adaptive frequency control strategy enables the RVPW011 to maintain high efficiency and tight regulation across a wide load range while minimizing EMI and power loss under light-load and no-load conditions.

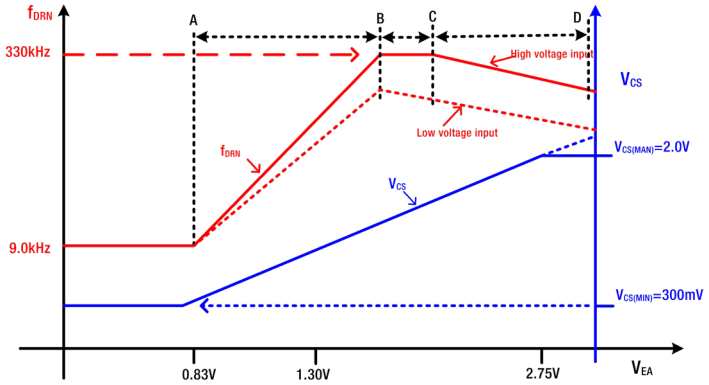


Fig. 16 Variation curves of switching frequency and peak current modulation with V_{EA}

Peak Current Setting of Power MOSFET

The peak current of power MOSFET NM0 in RVPW011 is controlled by a current modulator, which modulates the current I_{CS} generated by the voltage at VCS [3] pin and the external resistor R_{CS}, the current of the power MOSFET is 50000 times that of I_{CS}.
The value of R_{CS} can be calculated using the following formula:

$$R_{CS} = 50000 \times \frac{V_{CS(MAX)}}{I_{PK}}$$

Among them: $V_{CS(MAX)}$ is the maximum threshold voltage of VCS pin,with a typical value of 2V;
I_{PK} is the maximum peak current of the primary winding of the flyback converter.

FB Pin PSR Feedback Voltage Sampling

RVPW011 detects the output voltage of the switching power supply indirectly through the auxiliary winding of the transformer. A sampling resistor connected to the FB pin is used to sense the voltage from the auxiliary winding. During the transformer demagnetization stage, this sampled voltage serves as the negative input to the internal error amplifier EA, while the positive input is a fixed reference voltage $V_{REF(REG)}$=2V. The EA then performs differential amplification between the sampled voltage and the reference voltage to generate the duty cycle modulation voltage V_{EA}, which in turn adjusts the converter's duty cycle. As illustrated in Figure 17, the duty cycle is dynamically modulated by V_{EA} based on the error signal. The corresponding voltage waveform of the auxiliary winding during this process is shown in Figure 18. Once the feedback loop reaches a stable state, the sampled voltage at the FB pin matches the 2V reference of the error amplifier. At this point, the steady-state relationship between the output voltage and the auxiliary winding voltage can be used to calculate the output voltage as follows:

$$V_{FB} = (V_{OUT} + V_F + I_S R_S) \times \frac{N_A}{N_S} \times \frac{R_{FB1}}{R_{FB1} + R_{FB2}} = 2V$$

Thus, $$V_{OUT} = \frac{N_S}{N_A} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times 2V - (V_F + I_S R_S)$$

N_S and N_A represent the number of turns on the transformer's secondary output winding and primary auxiliary winding, respectively. R_{FB1} and R_{FB2} are the resistor divider components connected to the auxiliary winding for sampling, while V_F is the forward voltage drop of the output diode. I_S is the secondary-side output current, and R_S represents the total resistance of the secondary output circuit. From the output voltage expression, it is evident that the product I_SR_S impacts the load regulation of the switching power supply. To minimize this effect, the RVPW011 samples the FB pin voltage at the end of the demagnetization phase, when the secondary current I_S is at its lowest. In Discontinuous Conduction Mode (DCM), when I_S=0, the output voltage is no longer influenced by the I_SR_S term, thus significantly improving voltage accuracy. Therefore, for applications requiring high output voltage precision, it is recommended to design the converter to operate in DCM. In contrast, during Continuous Conduction Mode (CCM), the output voltage tends to decrease with increasing load due to the I_SR_S influence. RVPW011 detects the end of the demagnetization stage by monitoring the FB pin. A 20% drop in FB voltage is used as the trigger condition to latch the output of the internal error amplifier (EA). Since the EA output includes a built-in delay, the latched voltage reflects the FB level just before the sudden voltage drop occurs. At the beginning of the demagnetization period, resonance between the transformer's leakage inductance and parasitic capacitance can cause voltage fluctuations on the FB pin. To avoid incorrect sampling during this time, the device introduces a sampling delay $T_{D(SAMP)}$, during which the sampler is disabled. Sampling is only performed during a defined window T_{SAMP}, and during this period, the peak-to-peak resonance voltage on FB should be limited to within 20% (approximately 400mV) of the FB steady-state level. When translating this voltage back to the auxiliary winding side, the resistor divider ratio must be taken into account. It is important to avoid placing a filter capacitor from the FB pin to ground, as this can distort the FB waveform and degrade voltage regulation accuracy-particularly in high-frequency designs (e.g., 100s of kHz). Additionally, due to the short demagnetization duration at light loads, the parasitic capacitance of an oscilloscope probe may also alter the FB waveform during testing, potentially leading to output voltage instability. To ensure an optimal balance between signal integrity and power loss in the FB resistor network, it is recommended to select R_{FB1} in the range of 2.5kΩ to 10kΩ, with a typical value of 6kΩ. Care must be taken to ensure that the negative current flowing into the FB pin during transformer excitation does not exceed 2mA to avoid affecting device performance or damaging the internal circuitry.

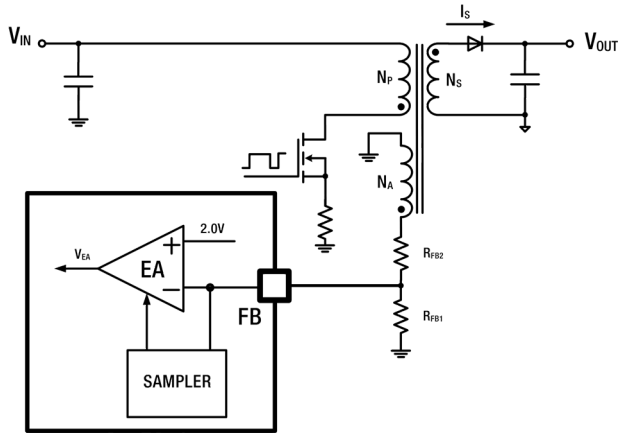


Fig. 17

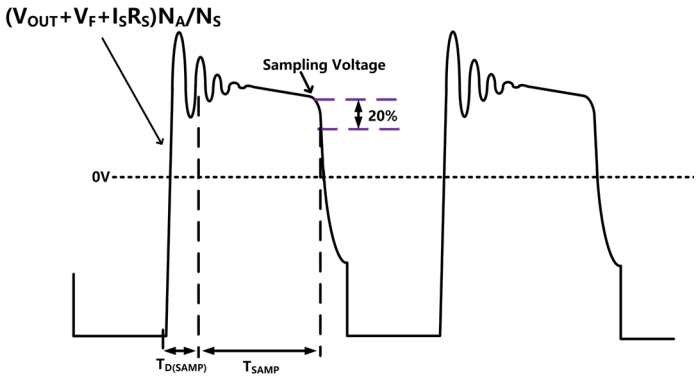


Fig. 18

Output Diode Temperature Compensation

RVPW011 features a temperature compensation selection function, illustrated in Figure 19. A positive temperature coefficient voltage, V_{TC}, is generated and processed through a unity gain amplifier to build drive capability. This voltage is then connected to the FB pin via a compensation resistor R_{TC}= 100kΩ. The V_{TC} exhibits a positive temperature coefficient of 3.5 mV/°C and equals the reference voltage $V_{REF(REG)}$ at room temperature. This arrangement enables the RVPW011 to perform temperature compensation in primary-side feedback flyback power supply applications. The magnitude of the temperature compensation effect is determined by the value of the voltage divider resistor R_{FB2}, which can be calculated as follows:

$$V_{OUT} = \frac{N_S}{N_A} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times V_{REF(REG)} - \{\frac{N_S}{N_A} \times \frac{R_{FB2}}{R_{TC}} \left[V_{TC} - V_{REF(REG)}\right] + V_D\}$$

In the above equation, N_S and N_A are respectively the turns of the secondary winding and auxiliary winding of the transformer, and V_D is the voltage drop across the output diode junction. To make the temperature coefficient of the output voltage small, taking the derivative of temperature to zero yields:

$$R_{FB2} = \frac{N_A}{N_S} \times \frac{\triangle V_D}{577.5mV} \times 100k\Omega$$

ΔV_D is the change in voltage drop of the output diode of the switching power supply from -40~125°C.Determine the size of R_{FB2} based on the temperature change value of the output diode junction voltage drop and the transformer turn ratio, and then determine the size of R_{FB1} based on the output voltage.

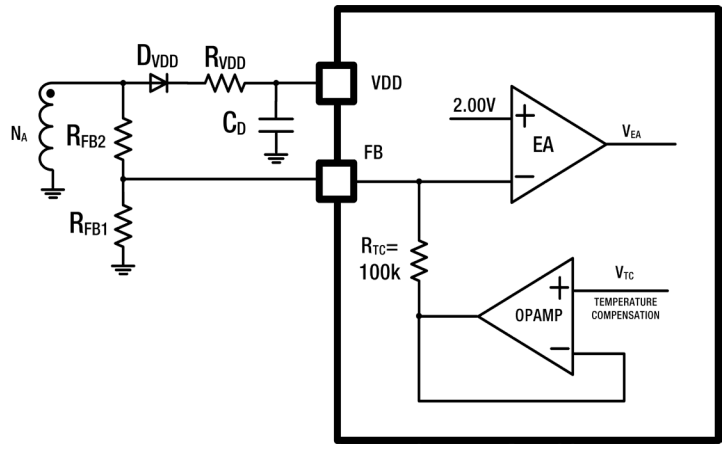
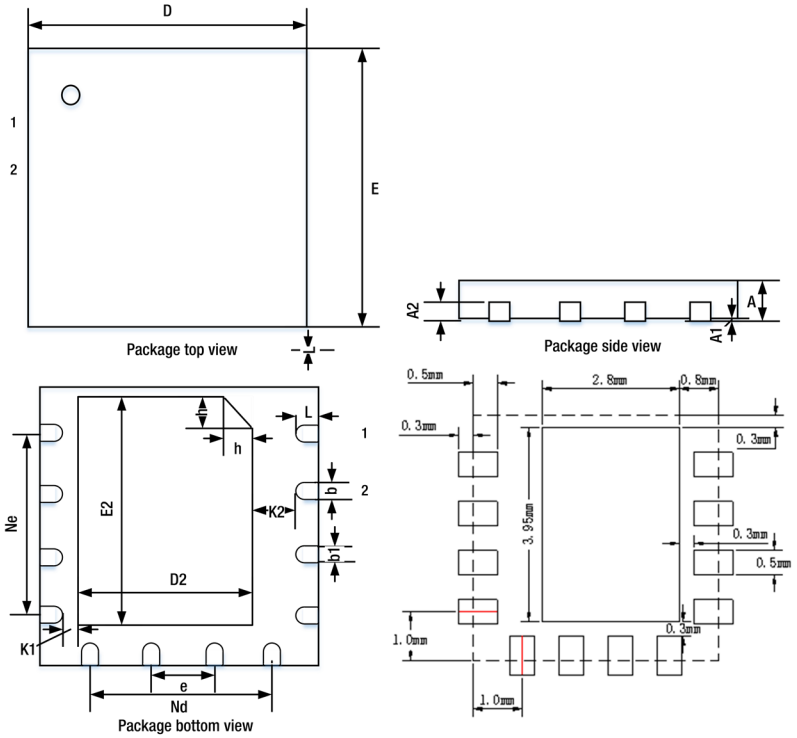


Fig. 19

PACKAGING INFORMATION

QFN5x5-12



DIMENSION TABLE			
SYMBOL	MILLIMETER		
	MINIMUM	NOMINAL	MAXIMUM
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2		0.203 REF	
b	0.25	0.30	0.35
b1	0.17	0.22	0.27
D	4.90	5.00	5.10
D2	2.70	2.80	2.90
Ne		3.00 BSC	
e		1.00 BSC	
E	4.90	5.00	5.10
E2	3.85	3.95	4.05
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K1	0.35	0.40	0.45
K2	0.95	1.00	1.05

ORDER INFORMATION

Device	Package Type	PIN	Packaging Method	QTY	Marking Code*	MSL
RVPW011-FJ1-R	QFN5x5	12	Tape and Reel	4000	RVPW011	MSL-3

*Marking Code:
RVPW011—— Product Code