RVP6501 Transformer Drivers for Micro-power Isolated Supplies

2.8-6VIN/24V/0.5A LDMOS

FEATURES

- Push-pull Topology
- Highly Integration Compatible with Simple Peripheries
- Built-in 24V/0.3Ω LDMOS
- 0.8A Current-limit
- Wide Input Voltage Range 2.8-6V
- Short Circuit Protection, Thermal Shut Down, Self Recovery
- Operating Temperature -40°C~+125°C

APPLICATIONS

- Isolated Power Supplies for CAN, RS-485, RS-232, SPI, I2C, etc.
- Process Control
- Precision/Medical Instrument
- Distributed/Radio/Telecom Power Supplies
- Low-noise Isolated USB Power Supplies
- Low-noise Filament Power Supplies
- IGBT Gate Drive Supplies

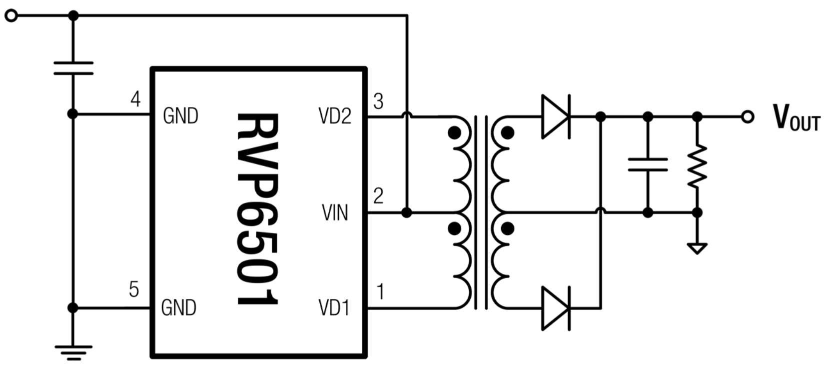
DESCRIPTION

RVP6501 is a Push-Pull transformer driver specifically designed for compact, isolated micropower supply applications requiring low standby power consumption. With minimal external components-namely a simple input/output filter capacitor, an isolated transformer, and a rectifier circuit-the RVP6501 enables the implementation of isolated power supplies with input voltages of 3.3V or 5V, output voltages ranging from 3.3V to 24V, and output power levels of 1W to 2W. The device features an integrated oscillator that generates a pair of high-precision complementary signals to drive two N-channel MOSFETs. Its symmetrical internal architecture ensures precise switching balance between the power switches, effectively minimizing magnetic bias during operation. Additionally, the RVP6501 incorporates a high-accuracy dead-time control circuit that prevents cross-conduction by ensuring that both power switches are never on simultaneously under any operating condition.

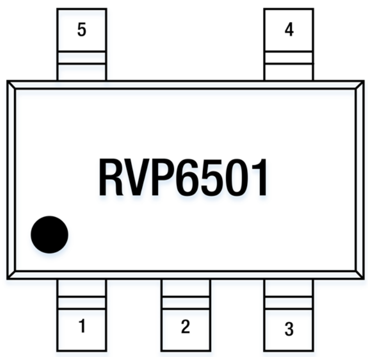
Device Information

Part Number	Package	Weight(mg)	Size	SPQ
RVP6501	SOT23-5	14.80	3.0 mm x 2.8 mm	3000

SIMPLIFIED SCHEMATIC



PIN CONFIGURATION AND FUNCTIONS



NAME	No.	TYPE	DESCRIPTION
VD1	1	O	Transformer driver output 1.
VIN	2	P	This is the device supply pin. It should be bypassed to GND with a 1µF capacitor mounted as close as possible to the device
VD2	3	O	Transformer driver output 2.
GND	4,5	P	Logic circuit grounding and analog circuit grounding.

RVP6501 Transformer Drivers for Micro-power Isolated Supplies

2.8-6VIN/24V/0.5A LDMOS

TECHNICAL SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
VIN Input Voltage	V_{IN}	-0.3	10	V
LDMOS Drain Voltage	VD1 , VD2	-0.3	24	
LDMOS Peak Current	$I_{(VD1)\ Pk}$, $I_{(VD2)\ PK}$		0.8	A
Maximum Junction Temperature	T_{JMAX}		150	°C
Storage Temperature Range	T_{STG}	-55	150	°C

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model (HBM), VD1 and VD2 to GND	±6000	V
		Other Pins, per ESDA/JEDEC JS-001-2017; (Zap 1 pulse, Interval :>=0.1S)	±2000	V
		Charged Device Model (CDM), per ESDA/JEDEC JS-002-2014	±1000	V

Thermal Resistance

Packaging	θ_{JA}	ψ_{JT}	UNIT
DFN2x2-6	210	11.2	°C/W

Note: Measured on a test board with 1oz copper (7.62cm × 11.43cm).

Recommended Operatings Conditions

		MIN	TYP	MAX	UNIT
VIN Input Voltage	V_{IN}	2.8		6	V
LDMOS Drain Voltage	I_{VD1}, I_{VD2}			0.5	A
Ambient Temperature	T_A	-40		125	°C

Electrical Characteristics

Unless otherwise noted, all values are at temperature T=25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN						
V_{IN}	Input voltage range		2.8		6.0	V
$V_{IN\ (ON)}$	Start Up Voltage	V_{IN} rising	2.4	2.65	2.8	V
$V_{IN\ (HYS)}$	Hysteresis voltage	V_{IN} falling		0.3		V
I_Q	V_{IN} quiescent current	VD1/VD2 floating		0.5	1.0	mA
VD1/ VD2						
DMM	VD1/VD2 pulse width mismatch ratio			0%		
$R_{DS(ON)}$	LDMOS on-resistance	VIN>3.5, I_{DS1} /I_{DS2}=0.2A, T=25°C		300	500	mΩ
		VIN>3.5V, I_{DS1} /I_{DS2} =0.2A, T=100°C		420	700	
V_{SLEW}	Voltage slew rate	VD1/VD2 are connected respectively with 50Ω to VIN		115		V/us
t_{BBM}	Interval between VD1 and VD2 (Break-before-make time)	VD1/VD2 are respectively connected with 50Ω to VIN, measuring I_{VIN}	120	175	230	ns
I_{LIM}	Initial value of Current Clamp Limit	VD1, VD2, VIN short connect	0.5	0.8		A
f_{SWO}	Operating frequency	VD1/VD2 are respectively connected with 50Ω to 5V	300	360	420	kHz

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUT DOWN PROTECTION						
T_{SHDN}	Thermal shut down threshold		146	167	178	°C
$T_{SHDN\ (HYS)}$	Thermal shut down hysteresis			15		°C

Typical Characteristics

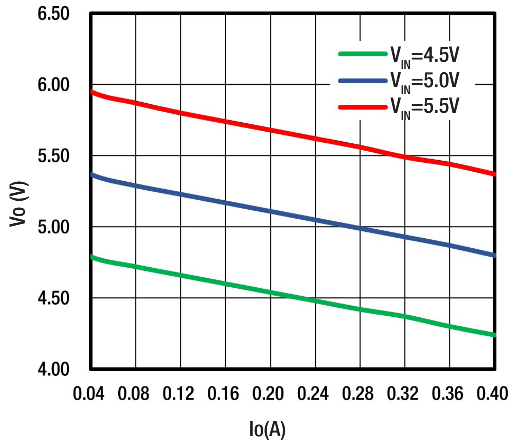


Fig. 1 Output Voltage vs Load Current (RVP6501+TMR-001-A55S, 5V to 5V/1W)

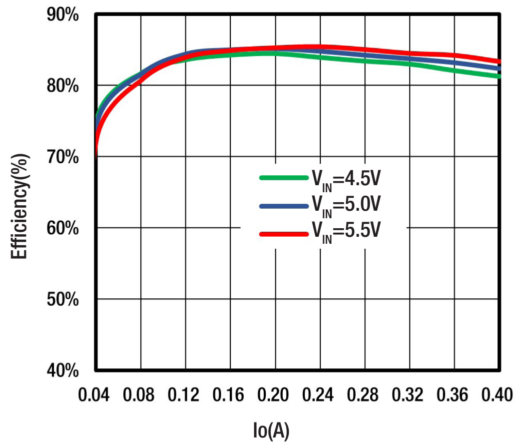


Fig. 2 Efficiency vs Load Current (RVP6501+TMR-001-A55S, 5V to 5V/1W)

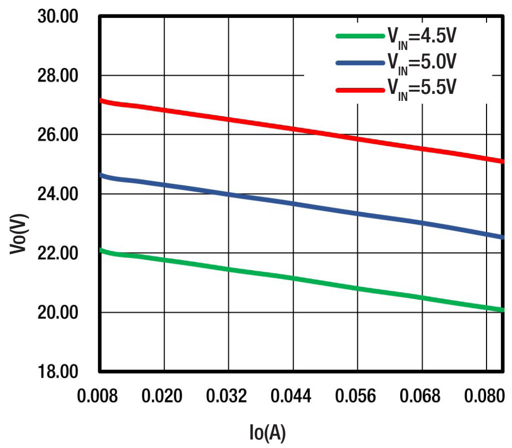


Fig 3. Output Voltage vs Load Current (RVP6501+TMR-002-C5BS, 5V to 24V/2W)

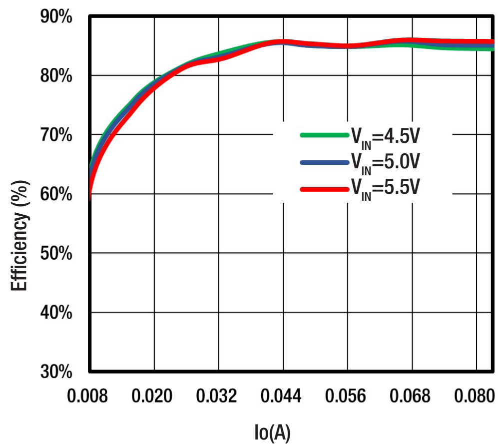


Fig 4. Efficiency vs Load Current (RVP6501+TMR-002-C5BS, 5V to 24V/2W)

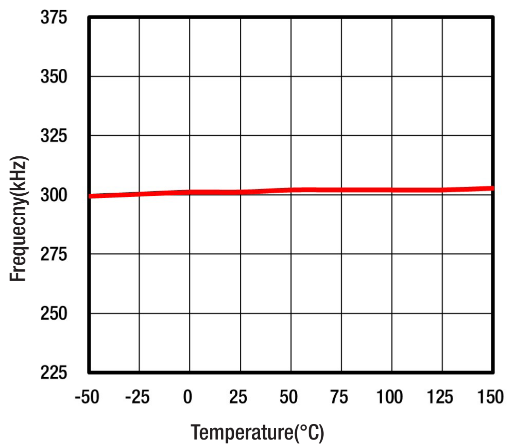


Fig. 5 Frequency vs Ambient Temperature

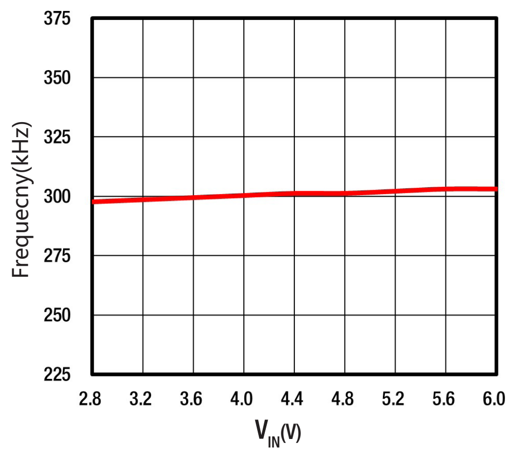


Fig 6. Frequency vs VIN

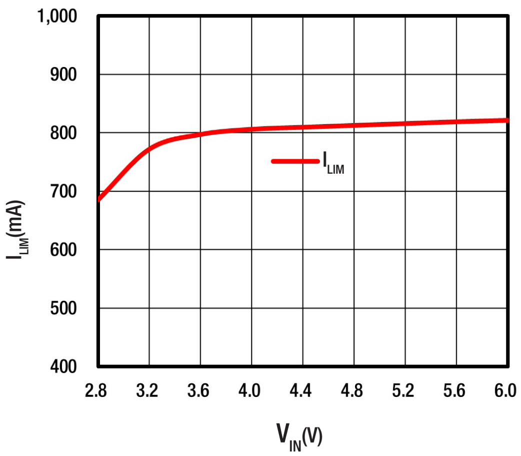


Fig. 7 Current Clamp limit vs Input voltage

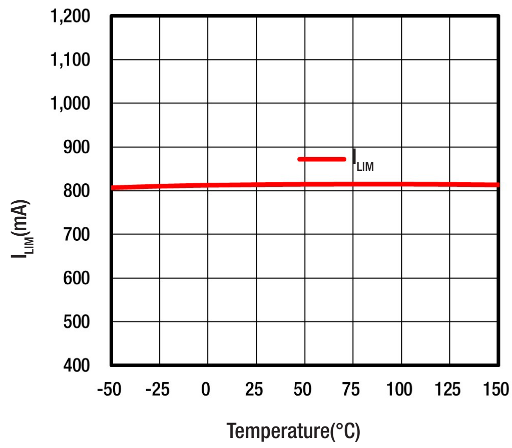


Fig. 8 Current Clamp limit vs Ambient Temperature

PARAMETER MEASUREMENT INFORMATION

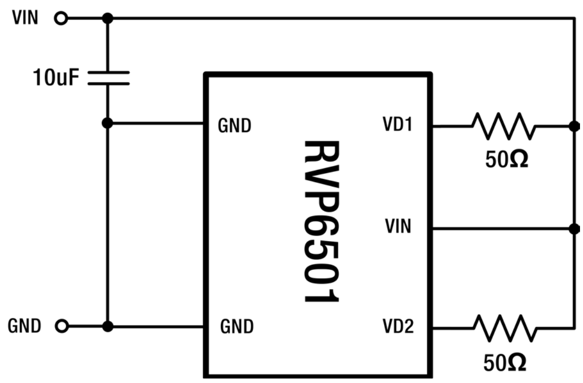


Fig. 9 Measurement Circuit f_{SW0}/ V_{SLEW}/ t_{BBM}

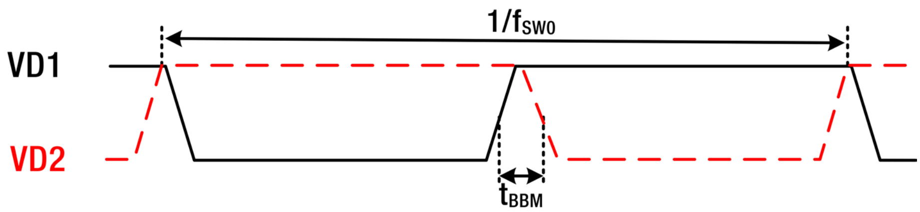


Fig. 10 Timing Diagram for VD1 and VD2

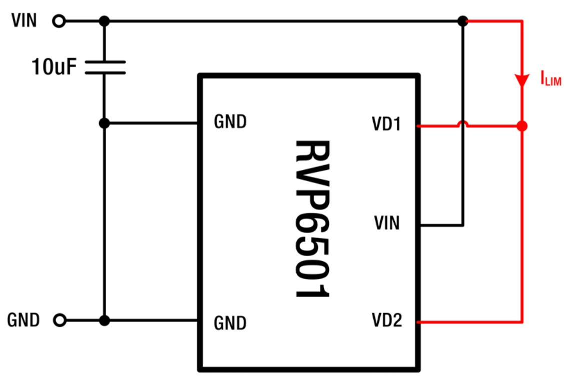


Fig. 11 I_{LIM} Measurement Circuit

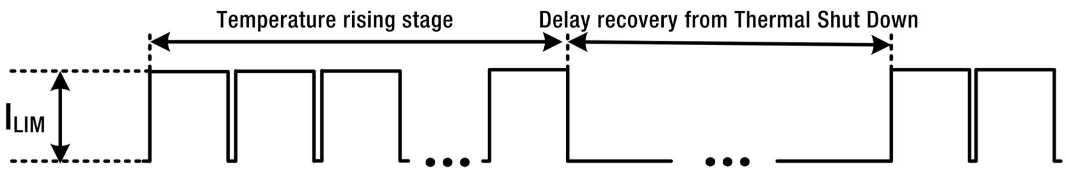


Fig. 12 Timing Diagram for I_{LIM}

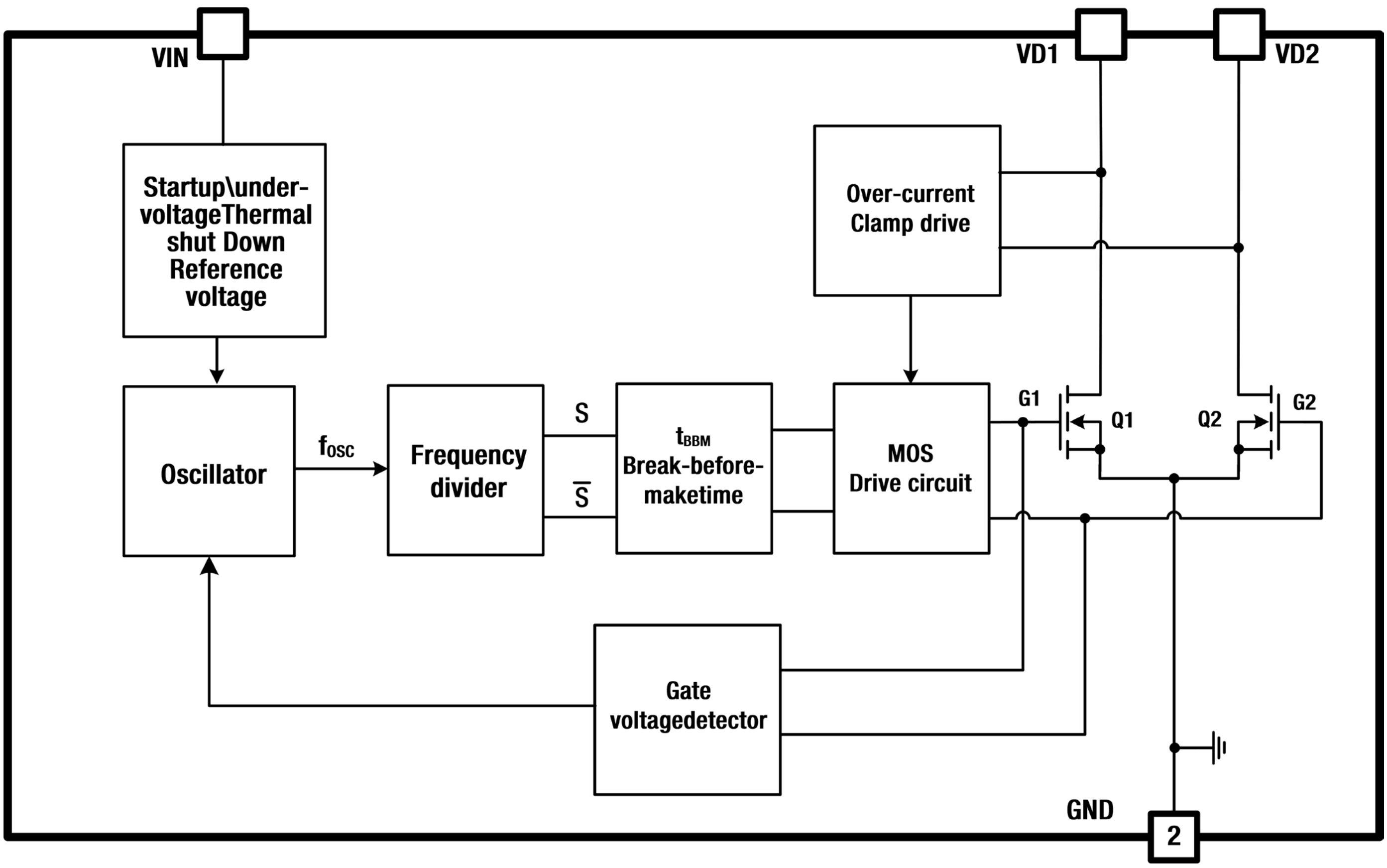
DETAILED DESCRIPTION

Overview

RVP6501 is an integrated Push-Pull controller specifically designed for isolated DC/DC switching power supply applications. It incorporates a pair of 0.3Ω nLDMOS power switches, supporting input voltage ranges from 2.8V to 6V. To ensure device protection and system reliability, an internal current-limiting mechanism clamps excessive current through the power switches. This not only maintains the chip's operation within a safe zone but also safeguards external components from high-current stress.

RVP6501 features a built-in oscillator, and includes a precisely engineered dead time (t_{BBM}) between the two gate drive signals to prevent simultaneous conduction of the power switches during switching transitions. This timing control also reduces the drain-source voltage at turn-on, thereby minimizing switching losses and improving overall efficiency.

Functional Block Diagram



Operating Principle

Push-pull Drive Sequence

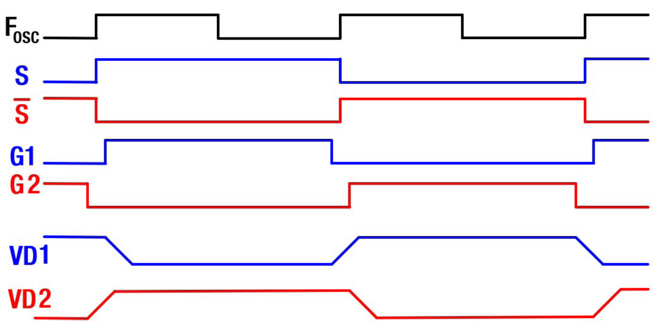


Fig. 13 Push-pull Drive Sequence and Output Signal Waveforms

As illustrated in Figure 13, the output signals G1 and G2 serve as gate drive signals for the LDMOS output transistors Q1 and Q2. Initially, both signals exhibit identical high-level pulse widths. Between these high pulses, a synchronized low-level interval is introduced-referred to as the break-before-make time (t_{BBM}). This interval prevents simultaneous conduction of both LDMOS channels, thereby avoiding shoot-through, reducing the drain voltage at turn-on, and minimizing switching losses. The gate voltage of Q1 and Q2 is actively monitored during shutdown. The t_{BBM} interval is generated only after the respective LDMOS has completely turned off, ensuring that drive timing is not affected by thermal coefficient variations. This approach maintains consistent dead-time control across the entire input voltage range, improving reliability and performance in demanding applications.

Current Clamp Drive Mode

Excessive current through the LDMOS transistors may be detected during converter startup, output short circuits, or transformer magnetic saturation. In such cases, the gate drive voltage of Q1 and Q2 is reduced to limit the current to a predefined Current Clamp Limit. This mechanism ensures that the LDMOS devices operate within a safe area, while also protecting the transformer and output rectifier diode from the damaging effects of high inrush currents. As a result, the overall reliability and robustness of the converter are significantly enhanced.

Thermal Protection

RVP6501 features integrated overtemperature protection with a typical shutdown threshold of 167°C. When the chip's junction temperature exceeds this threshold, the device enters a protection state by disabling the internal oscillator, effectively halting operation. Normal functionality is automatically restored once the junction temperature drops below the typical recovery threshold of 152°C. This thermal protection mechanism helps prevent damage due to overheating and ensures safe and reliable operation under varying thermal conditions.

Output Short Circuit Protection

RVP6501 implements output short-circuit protection through a combination of Current Clamp Drive Mode and Overtemperature Protection. When the output of the Push-Pull converter is short-circuited, the transformer's primary winding experiences minimal voltage drop, as most of the input voltage V_{IN} is absorbed by the conducting N-channel LDMOS transistor (Q1 or Q2). Upon detecting excessive current through the LDMOS, the device transitions into Current Clamp Drive Mode, limiting the current to a safe level. As current continues to flow, power dissipation in the LDMOS causes the junction temperature to rise. Once the internal temperature reaches the thermal shutdown threshold, the device enters Thermal Shutdown Protection Mode to prevent damage. Notably, lower ambient temperatures or reduced input voltages slow the rate of temperature increase, thereby extending the time before thermal shutdown occurs. This behavior enhances the converter's ability to handle large capacitive loads under short-circuit conditions, offering improved robustness and adaptive protection.

General Operating Mode

During startup, the output voltage of the converter is initially low, resulting in a high current through the LDMOS transistors. To ensure safe operation, the RVP6501 begins this stage in Current Clamp Drive Mode, limiting the current to protect both the device and external components. As the output voltage approaches its rated level, the current through the LDMOS decreases. At this point, the gate drive voltage is increased to reduce the internal on-resistance, thereby improving conduction efficiency and minimizing power loss.

Push-Pull Converter

Working Principle of a Push-Pull Converter

As shown in Figure 14, the Push-Pull converter primarily consists of switching transistors Q1 and Q2, an isolated center-tapped transformer TR1, a full-wave rectifier circuit formed by diodes D1 and D2, and input/output filter capacitors. During operation, switches Q1 and Q2 alternate conduction, generating AC voltages with opposite phases across the primary windings Np1 and Np2 of the transformer. These voltages are magnetically coupled and transferred to the secondary side via transformer TR1. On the secondary side, the full-wave rectifier formed by D1 and D2 converts the AC signal into a pulsating DC voltage, whose amplitude is determined by the transformer's turns ratio. This voltage is then filtered by the output capacitor Cout to produce a relatively stable DC output.

Because the Push-Pull topology transfers energy to the secondary side with a near-100% effective duty cycle, it achieves high conversion efficiency and strong dynamic performance. In theory, only a small output capacitor is required to achieve low ripple, thanks to the continuous energy transfer. However, to prevent simultaneous conduction of Q1 and Q2-which would short both ends of the transformer's primary-the controller introduces a break-before-make time between switching transitions. During this interval, the transformer does not supply power to the load, and the output capacitor temporarily provides the required energy. As a result, some degree of output voltage ripple is inevitable during this period.

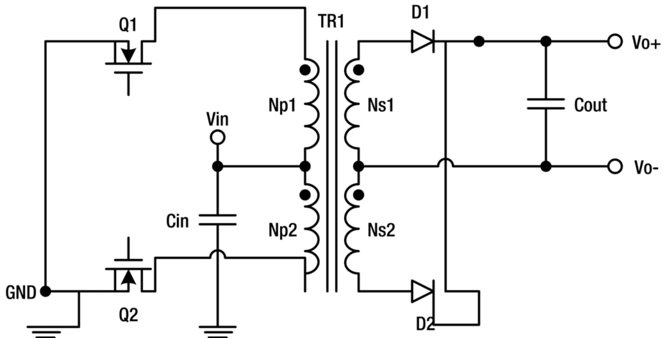


Fig. 14 Schematic Diagram of a Push-Pull Converter

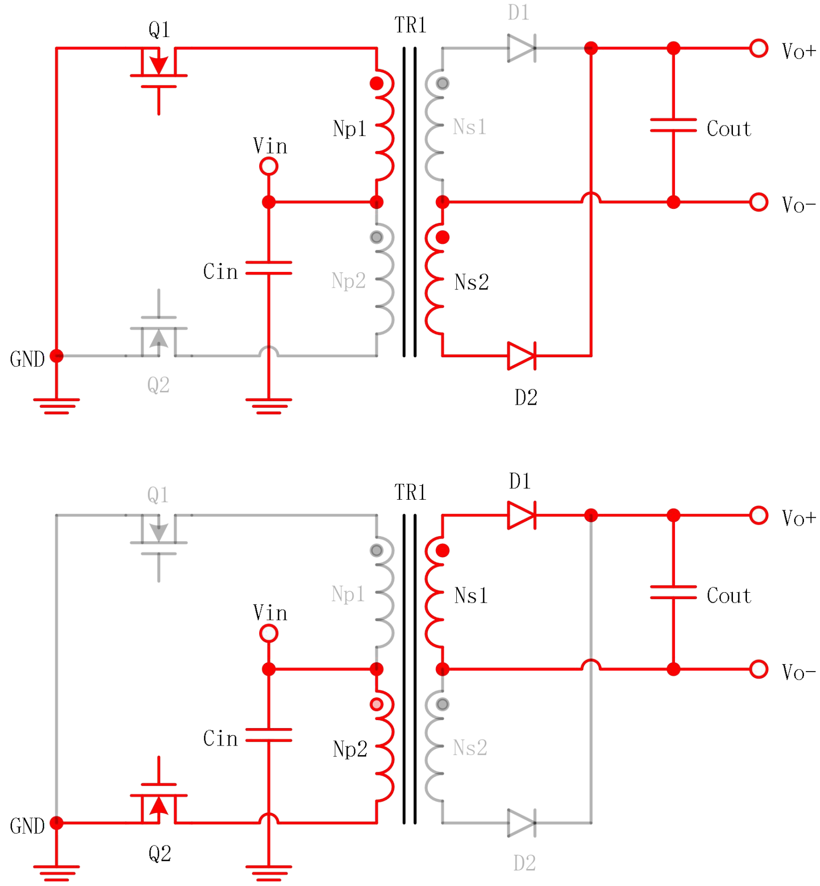


Fig. 15 Switching Cycles of a Push-Pull Converter

Figure 15 illustrates the equivalent schematic diagram of the Push-Pull converter's operating principle. Switches Q1 and Q2 operate alternately with an approximate 50% duty cycle. When Q1 is conducting, the input voltage Vin drives current from the un-dotted end of the primary winding Np1, through the upper half of the transformer's primary, exiting via the dotted end and flowing through Q1 to ground. During this conduction phase, energy is transferred to the secondary side of the transformer TR1. According to Faraday's Law of Electromagnetic Induction, while Q1 conducts, an induced voltage appears on the secondary winding Ns2. Current flows out from the un-dotted end of Ns2, passes through rectifier diode D2, delivers power to the output terminal V_{0+}, flows through the load, and returns to the dotted end of Ns2 via V_{0-}. The operation during Q2 conduction mirrors that of Q1 and is not elaborated further here for brevity. During alternating conduction, voltages are induced across all transformer windings (Np1, Np2, Ns1, and Ns2). The amplitude of these induced voltages is directly proportional to the transformer's turns ratio and follows the rule of identical polarity at corresponding winding ends. Assuming ideal components (i.e., Q1, Q2, D1, and D2 without parasitic effects), it can be concluded that the drain voltage of Q1 and Q2 can reach up to twice the input voltage Vin, while the reverse voltage across D1 and D2 can reach twice the output voltage Vo during operation.

Core Magnetization

For the Push-Pull transformer to operate normally and avoid core saturation, it must satisfy the principle of volt-second balance. This means that the product of voltage and time (volt-seconds) applied during the excitation phase must be equal to the product of volt-seconds during the demagnetization phase. Any imbalance between these two phases can result in the accumulation of magnetic flux and ultimately cause core saturation.

Figure 16 illustrates the magnetization curve of a Push-Pull converter, where B represents magnetic flux density and H represents magnetic field strength. When switch Q1 is conducting, the transformer enters the excitation phase, driving the magnetic flux from point A to point A'. Conversely, when switch Q2 conducts, the transformer enters the demagnetization phase, during which the magnetic flux is drawn back from A' to A, resulting in a gradual decrease in flux density. This alternating process ensures the magnetic core returns to its original state each cycle, maintaining stability and preventing saturation.

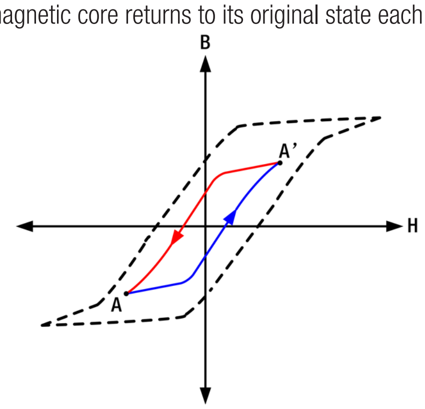


Fig. 16 Core Magnetization Cure of a Push-Pull Transformer

At the moment switch Q2 turns off, the magnetic flux density B in the transformer reaches its negative maximum. The magnitude of B is primarily determined by the product of the voltage amplitude V_P applied to the primary winding and the switch-on duration Ton, commonly referred to as the volt-second product. For stable operation, a Push-Pull transformer must adhere to the volt-second balance principle: the volt-second product during the excitation phase must equal that during the demagnetization phase. If this balance is not maintained, the volt-second values during the two switching phases differ-an imbalance in magnetic flux results, causing the B-H operating point to shift away from the origin. If uncorrected, this shift accumulates cycle by cycle, gradually driving the transformer core toward saturation, ultimately leading to abnormal operation. In practical applications, where MOS transistors are used as the main switching devices, an inherent deviation correction mechanism helps mitigate this effect. Due to unavoidable asymmetries in switch timing, the on times of Q1 and Q2 may not be perfectly equal, leading to minor discrepancies in the transformer's volt-second balance and causing magnetic bias. This bias increases the current in the corresponding switch path, raising conduction losses and thermal stress. However, because MOSFETs exhibit a positive temperature coefficient in their on-resistance $R_{DS(on)}$, the increased temperature leads to higher voltage drops across the conducting switch. This in turn reduces the effective voltage V_P applied to the transformer winding during conduction. As a result, the volt-second imbalance is automatically mitigated over time, providing a self-correcting mechanism that helps maintain magnetic balance and improves long-term operating stability.

TYPICAL APPLICATION

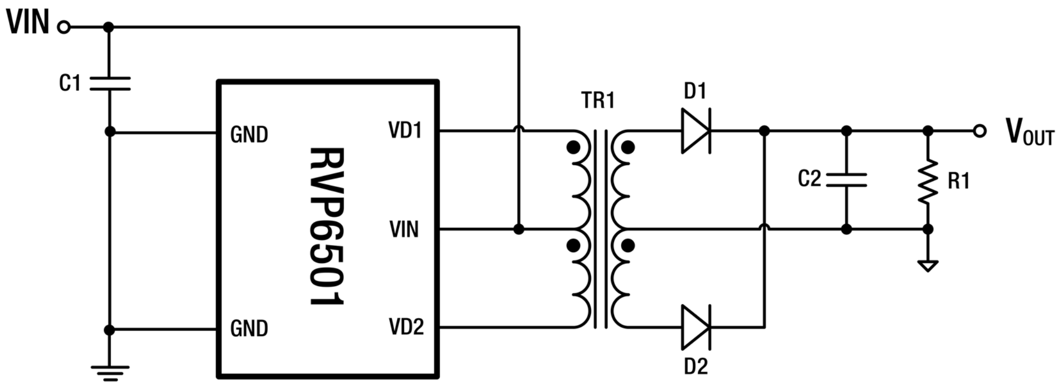


Fig. 17 Typical Application Schematic

Design Requirements

The following applications are typical ones based on the input voltage of 5V ± 10%, isolated non regulated 5V output, and maximum output power of 1W. The relevant technical parameters of the power supply are shown in the table below:

Input and Output Parameters

TECHNICAL SPECIFICATION	MIN	TYP	MAX	UNIT
Input Voltage	4.5	5.0	5.5	V
Output Voltage	---	5.0	---	V
Output Current	---	0.2	---	A
Output Ripple + Noise	---	50	100	mV
Voltage Regulation Rate	---	---	1.5	%
Load Regulation Rate	---	---	10	%
Efficiency	---	85	---	%
Reliability Requirements				
Output Short Circuit Protection	Continuous, self-recovery			
Operating Temperature	-40	---	85	°C
Isolation Withstand Voltage	1500	---	---	VDC

Input Capacitor Selection

As shown in Figure 17, the input capacitor C1 serves multiple purposes, including energy storage, filtering, and decoupling. To enhance high-frequency decoupling, an additional 0.1µF ceramic capacitor may be connected in parallel between VIN and GND, placed as close to the device as possible. During the operation of the Push-Pull converter, capacitor C1 supplies transient current to the converter, helping to stabilize input voltage and reduce ripple. For optimal performance, it is recommended to use a capacitor with a capacitance in the range of 1µF to 10µF, depending on the load and input conditions. The capacitor's voltage rating must exceed the maximum input voltage with sufficient margin to account for voltage derating. A surface-mount ceramic capacitor with low equivalent series resistance (ESR) and stable temperature characteristics is strongly recommended. To maximize filtering effectiveness and minimize electromagnetic interference (EMI) and voltage spikes, capacitor C1 should be placed as close as possible to the device's power input pins. Additionally, all power traces-particularly those connecting the input capacitor-should be kept short and wide to reduce parasitic inductance and resistive losses, which can cause unwanted voltage transients during switching events.

Output Rectifier Diode Selection

Schottky diodes, which feature low forward voltage drop and fast recovery time, are recommended for use in the output rectifier stage of the Push-Pull converter. These characteristics contribute to improved load regulation and higher overall conversion efficiency. The application circuit adopts a full-wave rectifier structure at the output. In this topology, the reverse voltage stress on each rectifier diode can reach approximately twice the output voltage. Therefore, the selected diode must have a reverse voltage rating greater than twice the maximum expected output voltage, which should be calculated based on the highest input voltage and minimum load conditions. Appropriate voltage derating should also be applied to ensure long-term reliability. It is essential that the selected rectifier diode is rated for the full range of expected operating temperatures. At elevated temperatures, the reverse leakage current of Schottky diodes increases significantly, which may impact efficiency and thermal stability. As such, temperature-dependent behavior must be taken into account, and suitable derating should be applied. Designers are advised to consult the temperature derating curves provided in the diode manufacturer's specification to ensure reliable operation at high temperatures.

To guarantee robust and stable performance under all operating conditions, including fault scenarios such as an output short circuit, the rectifier diode must also be selected to handle the maximum current stress. When the RVP6501 detects a short circuit at the output, it automatically enters Output Short-Circuit Protection Mode and transitions to Current Clamp Drive Mode. In this state, the internal circuitry limits the current flowing through the primary-side MOSFETs to a defined Current Clamp Limit, which typically is 0.8 A. At this point, the output current seen by the rectifier diode depends on the transformer's turns ratio. At this time, the maximum working current of the output rectifier diode can be obtained according to turns ratio of the transformer, which can be calculated with the following formula:

$$I_{D-MAX} = \frac{N_P}{N_S} \times I_{LIM-MAX}$$

Where N_P is the number of turns of the primary winding of the Push-Pull transformer, N_S is the number of turns of the secondary winding, and $I_{LIM-MAX}$ is the maximum current clamp limit of the device.

When the RVP6501 enters Output Short Circuit Protection Mode, it first switches to Current Clamp Drive Mode. As the power dissipation within the device increases, it subsequently triggers Thermal Shutdown Protection Mode. During the interval from entering the self-recovery process until the activation of thermal shutdown, the output rectifier diode experiences its maximum current stress. Therefore, when selecting the output rectifier diode, it is critical to ensure that the diode's peak forward surge current rating (I_{FSM})meets or exceeds this requirement.

In this application, the Schottky diode with part number RB160M-30 is chosen. At an operating temperature of 75°C, this diode exhibits a forward conduction voltage drop of approximately 280mV@0.2A and a reverse leakage current of around 90µA@15V. Its peak forward surge current rating is 30A. For designs requiring higher operating temperatures, Schottky diodes with lower reverse leakage currents at elevated temperatures should be considered to maintain efficiency and reliability.

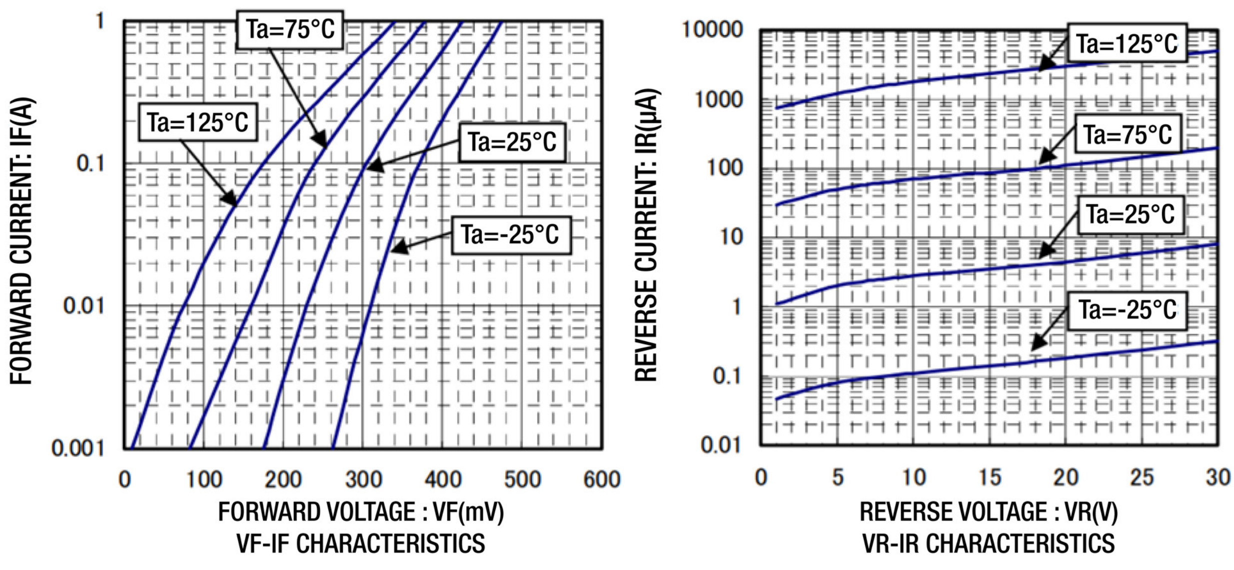


Fig. 18 Operating Characteristic of Schottky Diode RB160M-30

Output Capacitor Selection

The Push-Pull converter can theoretically transfer energy to the secondary winding at a 100% duty cycle. However, to ensure reliable operation, a break-before-make interval must be incorporated during the switching transitions between MOSFETs Q1 and Q2 to prevent both switches from conducting simultaneously, which would cause a short circuit. During this break-before-make period, the output energy is primarily supplied by the output filter capacitor C2, resulting in a temporary output voltage ripple. In practical applications, it is recommended to use a low-ESR ceramic capacitor with a capacitance between 4.7µF and 10µF for capacitor C2 to achieve improved filtering performance and minimize output ripple.

Push-Pull Transformer Selection

Estimation of Turns Ratio of the Primary and the Secondary: Assuming that the output rectifier diode of the Push-Pull converter has been selected in accordance with the design requirements, the forward conduction voltage drop V_F of the diode under maximum output load conditions can be determined. The turns ratio between the primary and secondary windings of the Push-Pull transformer can then be estimated based on the input voltage applied to the primary winding and the minimum output voltage required at the secondary winding. Under the nominal input and full load output, the input voltage at both ends of the primary winding of the Push-Pull transformer is:

$$V_P = V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} \times R_{DS(ON)}$$

Where P_{O-MAX} is the maximum output power of the Push-Pull converter, η is estimiated efficiency, V_{IN} is the nominal input, $R_{DS(ON)}$ is the on-resistance of the built-in N-MOS transistor in the device.
Under the condition of full load output, the minimum output voltage of the secondary winding is:

$$V_S = V_{O-MIN} + V_F$$

Where V_{O-MIN} is the minimum output voltage allowed by the Push-Pull converter under full load conditions. To ensure that the output voltage meets the specified requirements under full load, V_{O-MIN} can be estimated as 97% of the nominal output voltage, accounting for a tolerance of -3% from the nominal value. V_F represents the forward conduction voltage drop of the selected output rectifier diode under full load conditions. Calculation formula of turns ratio of the primary and the secondary windings can be obtained from the formula above:

$$N_{PS} = \frac{V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} \times R_{DS(ON)}}{V_{O-MIN} + V_F}$$

According to the input and output requirements of this application, assuming that the efficiency of the Push-Pull converter is 85%, it can be estimated that the turns ratio of the primary and the secondary windings of the Push-Pull transformer is:

$$N_{PS} = \frac{5V - \frac{1W}{0.85 \times 5V} \times (0.3\Omega)}{5V \times 0.97 + 0.34V} \approx 0.95$$

V-t Product Calculation for the Push-Pull Converter

To prevent transformer saturation, its volt-second V-t product rating must exceed the maximum V-t product applied during normal operation. When specifying the input parameters for the isolated power supply, a typical input voltage range of ±10% around the nominal value is considered. Consequently, the volt-second product of the Push-Pull transformer should be calculated based on the upper limit of the input voltage range. Additionally, the switching frequency and its tolerance, as defined by the device, must be taken into account to ensure that saturation does not occur even at the minimum operating frequency. The maximum volt-second product applied to the transformer's primary winding by the RVP6501 occurs when the device operates at its minimum switching frequency, which corresponds to half of the switching cycle, and at the maximum input voltage. Therefore, the following calculation methods can be taken as reference in the minimum volt second product estimation of the Push-Pull transformer:

$$V\mathrm{t}_{MIN} \geq V_{IN-MAX} \times \frac{T_{MAX}}{2} = \frac{V_{IN-MAX}}{2 \times f_{MIN}}$$

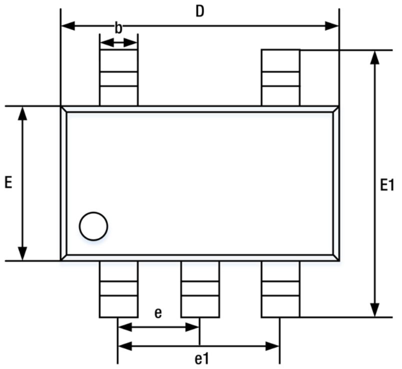
According to the design requirements of this application, assuming that the typical value of the operating frequency set is 360kHz and the minimum working frequency set is 300kHz. Under the highest input conditions, the volt second product of the selected Push-Pull transformer shall meet:

$$Vt_{MIN} \geq \frac{5V \times 110\%}{2 \times 300kHz} \approx 9.17V\mu s$$

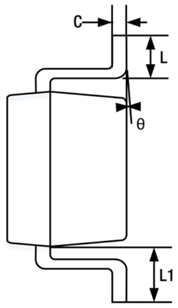
The selection of the Push-Pull transformer should be based on the appropriate volt-second product and the turns ratio between the primary and secondary windings, according to the specific application requirements. Additionally, factors such as the maximum output power, isolation voltage rating, and isolation distributed capacitance must also be carefully considered as important criteria during the selection process.

PACKAGING INFORMATION

SOT23-5

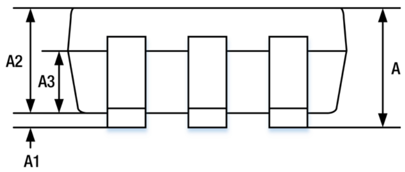


Package top view

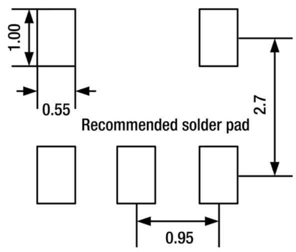


Package side view

DIMENSION TABLE			
SYMBOL	MILLIMETER		
	MINIMUM	NOMINAL	MAXIMUM
A	---	---	1.25
A1	0.04	---	0.12
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	---	0.50
C	0.14	---	0.20
D	2.82	2.92	3.02
E	1.50	1.60	1.70
E1	2.60	2.80	3.00
e	0.95 REF		
e1	1.90 REF		
L	0.35	0.45	0.60
L1	0.59 REF		
θ	0°	---	8°



Package front view



Recommended solder pad

ORDER INFORMATION

Device	Package Type	PIN	Packaging Method	QTY	Marking Code*	MSL
RVP6501-PPN-R	SOT23-5	5	Tape and Reel	3000	RVP6501	MSL-3

*Marking Code :
RVP6501—— Product Code

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