

RVP007 Transformer Driver for Isolated Supplies

4.5-24VIN ◇ 24V ◇ 1.2A Power MOSFET

FEATURES

- Full-bridge topology
- Supports LLC topology applications
- High level of integration with minimal external components
- Integrated 0.15Ω NMOS
- Integrated 0.30Ω PMOS
- 2.2A current clamp limit
- 4.5V to 24V input voltage range
- Input overvoltage protection
- Input surge voltage up to 38V
- Programmable operating frequency
- Enable shutdown function
- Integrated soft-start
- Continuous short-circuit protection and overtemperature protection with auto-recovery
- Operating temperature range: –40°C to +125°C

APPLICATIONS

- IGBT / SiC gate driver power supplies
- Auxiliary power supplies for isolated interfaces
- Precision instruments / medical equipment
- Auxiliary power supplies for DCS / PLC systems
- UPS systems and photovoltaic inverters
- Distributed power supplies / radio power supplies / telecommunication power supplies

DESCRIPTION

The RVP007 is a transformer driver specifically designed for compact, low standby power, medium- and low-power isolated power supplies. With only simple external input/output filter capacitors, an isolation transformer, and rectifier circuits, the device can realize isolated power supplies with 4.5V to 24V input voltage, multiple output voltage options, and output power ranging from 1W to 20W.

The RVP007 integrates two N-channel power MOSFETs and two P-channel power MOSFETs internally, configured in a bridge topology. An internal oscillator generates a pair of highly accurate complementary signals, effectively ensuring excellent symmetry between the two MOSFET drive paths and preventing transformer core bias during operation. For improved EMI performance and efficiency the device can be used in LLC configuration.

The operating frequency of the RVP007 can be selected through the CLK pin. If the CLK pin is left floating, the device operates at a fixed internal frequency of 250kHz. If a resistor is connected from CLK to GND, the operating frequency is programmed according to the resistor value.

The RVP007 also integrates a highly symmetrical dead-time control circuit to prevent shoot-through under various operating conditions. In addition, the device includes input overvoltage protection, overcurrent protection, and overtemperature protection to prevent device damage under abnormal conditions such as output short circuits in the switching power supply system.

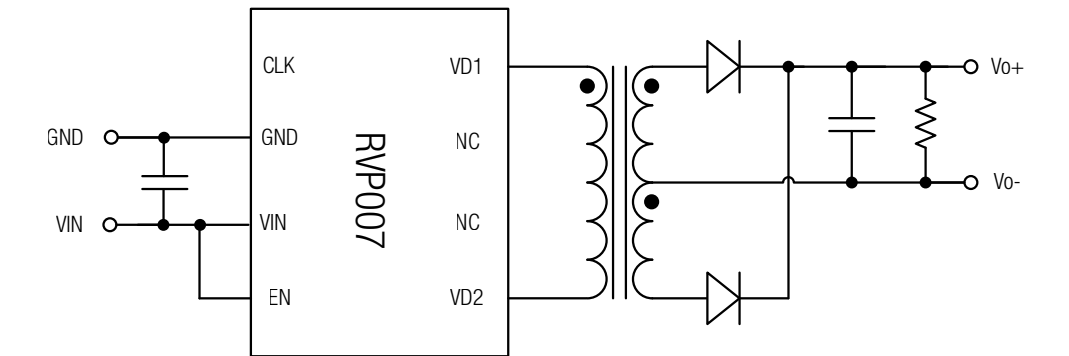
DEVICE INFORMATION

Part number	Package type	Dimension	SPQ
RVP007	ESOP8	5mm×6mm	4000

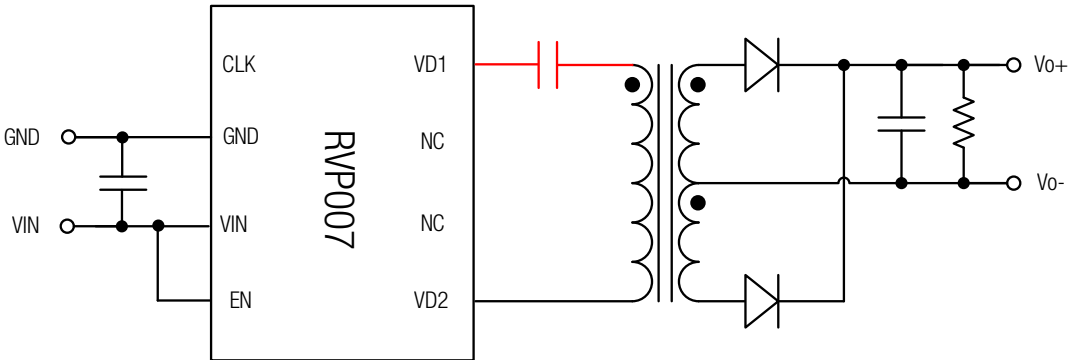
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SIMPLIFIED APPLICATION SCHEMATIC

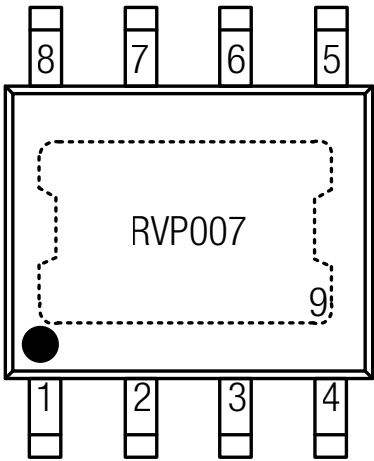
Full-bridge topology



LLC topology



PIN CONFIGURATION AND FUNCTIONS



Name	No.	Type	Description
CLK	1	I	Frequency setting pin. When CLK is held high (internally pulled high when left floating), the device automatically selects the internal fixed clock frequency of 250kHz. When a programming resistor R_{CLK} is connected from CLK to GND, the operating frequency can be programmed within the range of 75 kHz to 750 kHz. The approximate frequency programming formula is: $f_{SW} = 7500 / R_{CLK}$ (kHz), where R_{CLK} is in k Ω .
GND	2	P	Logic ground and analog ground.
VIN	3	P	Power supply input. Use a 1 μ F capacitor to bypass VIN to GND, and place the capacitor as close to the device as possible.

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Name	No.	Type	Description
EN	4	I	Enable pin. When this pin is pulled low, the device stops operating. When left floating or driven high, the device operates normally.
VD2	5	O	Transformer driver output 2.
NC	6,7	-	No-connect pin (NC pin).
VD1	8	O	Transformer driver output 1.
EP	9	P	Exposed pad (EP). Internally connected to GND, but not intended as an electrical connection point. Connect the EP to a large ground plane area to improve heat dissipation.

TECHNICAL SPECIFICATION**Absolute maximum ratings**

		Min.	Max.	Unit
VIN and EN pin voltage	V_{IN}, V_{EN}	-0.3	38	V
LDMOS drain voltage	V_{D1}, V_{D2}	-1.3	$V_{IN}+0.3$	V
	V_{D1}, V_{D2} (20 ns pulse duration)	-2.5		V
Peak current of the LDMOS power MOSFET	$I_{(VD1)PK}, I_{(VD2)PK}$		2.8	A
CLK pin voltage	V_{CLK}	-0.3	6.6	V
Maximum operating junction temperature	T_{JMAX}		150	°C
Storage temperature range	T_{STG}	-55	150	°C

Stress levels exceeding the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Prolonged exposure to absolute maximum rating conditions may affect device reliability. All voltages are referenced to ground. Currents are positive into and negative out of the specified terminal.

ESD ratings

		Value	Unit
$V_{(ESD)}$	ESD Ratings	Human Body Model (HBM), per ESDA/JEDEC JS-001-2017, (Zap 1 pulse, Interval: $\geq 0.1s$) ⁽¹⁾	± 3000 V
		Charged Device Model (CDM), per ESDA/JEDEC JS-002-2014 ⁽²⁾	± 1000 V

Note (1): JEDEC document JEP155 states that 500-V HBM allows safe manufacturing in standard ESD control processes.

Note (2): JEDEC document JEP157 states that 250-V CDM allows safe manufacturing in standard ESD control processes.

Recommended operations conditions

		Min.	Typ.	Max.	Unit
VIN input voltage	V_{IN}	4.5		24	V
LDMOS drain current	I_{VD1}, I_{VD2}			1.2	A
External programming resistor connected to the CLK pin	R_{CLK}	9		100	kΩ
Operating junction temperature	T_J	-40		125	°C

Thermal resistance information

Package	Parameter	Value	Unit
ESOP8	Junction-to-ambient thermal resistance R_{eJA}	52	°C/W
	Junction-to-case thermal resistance Ψ_{JT}	6.5	

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TECHNICAL SPECIFICATION**Electrical characteristics**(the following parameters are measured under the conditions of CLK left floating, $V_{IN} = 12V$ and $T_{AMB} = 25^{\circ}C$, unless otherwise stated)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input pin VIN						
V_{IN}	Input voltage range		4.5		24	V
$V_{IN(ON)}$	Startup voltage	EN floating, V_{IN} rising	3.2	3.6	4.2	V
$V_{IN(HYS)}$	Hysteresis voltage	EN floating, V_{IN} falling		0.4		V
$V_{IN(OVP)}$	Input overvoltage protection threshold	EN floating, V_{IN} rising	30	32.5	35	V
$V_{IN(OVP)(HYS)}$	Overvoltage protection hysteresis	EN floating, V_{IN} falling		17		mV
I_Q	VIN static current	V_{D1} , V_{D2} , CLK, and EN floating	2	2.8	4.7	mA
$I_{VIN(OFF)}$	VIN current after enable shutdown	EN = 0V		40	80	μA
Enable pin EN						
$V_{EN(ON)}$	EN enable turn-on voltage	V_{EN} voltage rising	0.6	0.9	1.2	V
$V_{EN(HYS)}$	EN enable shutdown hysteresis	V_{EN} voltage falling		80		mV
$I_{EN(SRC)}$	Current flowing out of the EN pin	V_{EN} voltage rising to $V_{EN(ON)} + 0.1 V$	26	43	60	μA
Output pins VD1/VD2						
DMM	VD1 / VD2 pulse width mismatch ratio			0%		
$R_{DSN(ON)}$	NMOS on-resistance	$T=25^{\circ}C$, $I_{DS}=0.5A$		0.15		Ω
		$T=100^{\circ}C$, $I_{DS}=0.5A$		0.2		Ω
$R_{DSP(ON)}$	PMOS on-resistance	$T=25^{\circ}C$, $I_{DS}=0.5A$		0.3		Ω
		$T=100^{\circ}C$, $I_{DS}=0.5A$		0.39		Ω
V_{SLEW}	Voltage slew rate	VD1 and VD2 each connected to GND through 240 Ω		192		V/ μS
t_{BBM}	VD1/ VD2 interval time	VD1 and VD2 each connected to GND through 240 Ω		109		ns
I_{LIM0}	Initial current clamp limit	1 Ω power resistor connected between VD1 and VD2, VIN = 4.5V, measuring the IVIN current magnitude	0.3	0.45	0.6	A
I_{LIM1}	Steady-state current clamp limit		1.5	2.2	2.7	A
t_{SS}	Time for ILIM0 to rise to ILIM1			3		mS
Frequency setting pin CLK						
f_{SW0}	Internal frequency	CLK floating	220	250	280	kHz
f_{SW1}	Programmable frequency	$R_{CLK} = 50 k\Omega$	135	155	175	kHz
V_{CLK}	CLK reference voltage	$R_{CLK} = 50 k\Omega$		1.27		V
Overtemperature protection threshold						
T_{SHDN}	Overtemperature protection threshold		145	162	178	$^{\circ}C$
$T_{SHDN(HYS)}$	Overtemperature protection hysteresis			17		$^{\circ}C$
$T_{OFFMIN(OTP)}$	Minimum shutdown time during overtemperature protection			2^{18}		T_{SW}

TECHNICAL SPECIFICATION

Typical characteristic curve

Figure 1. Operating frequency vs CLK programming resistor

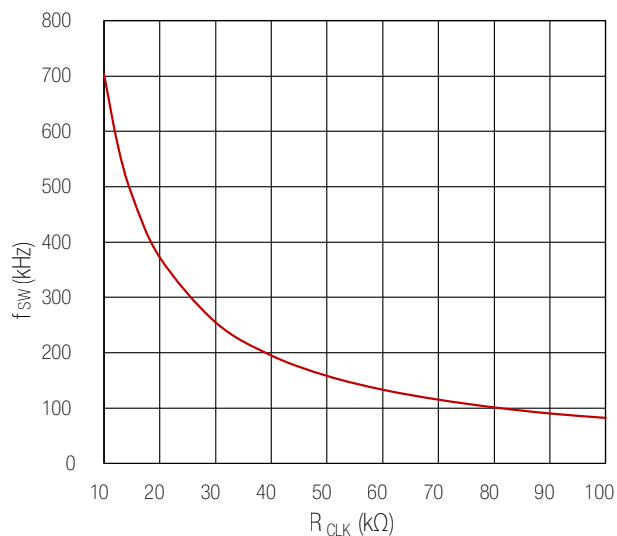


Figure 2. Operating frequency vs Temperature

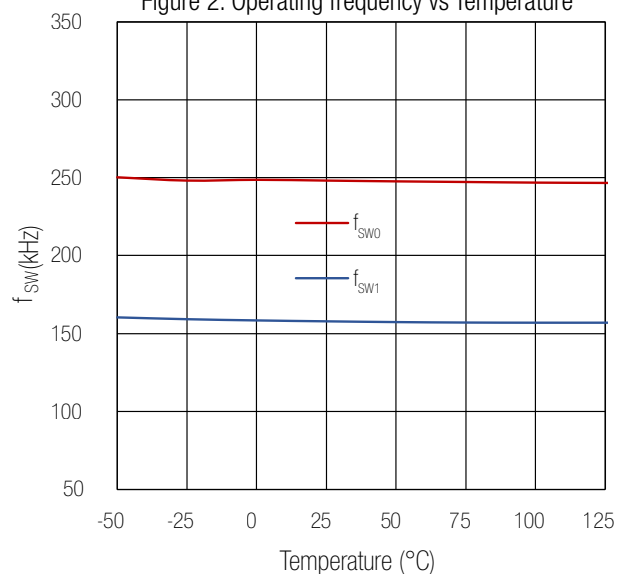


Figure 3. V_{EN} threshold voltage vs. temperature

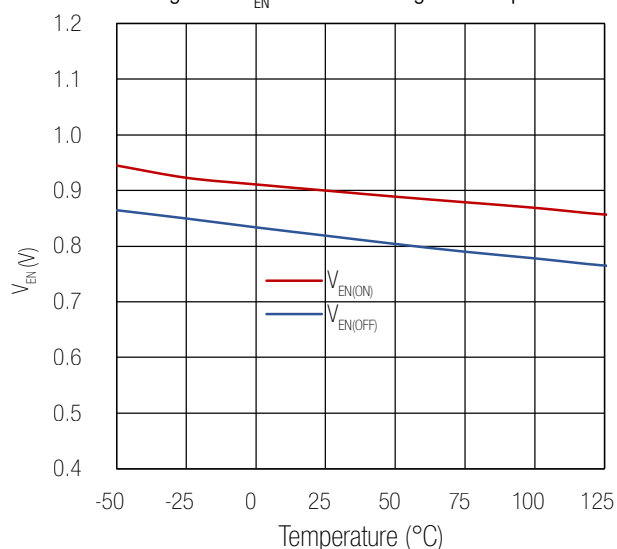


Figure 4. V_{IN} threshold voltage vs. temperature

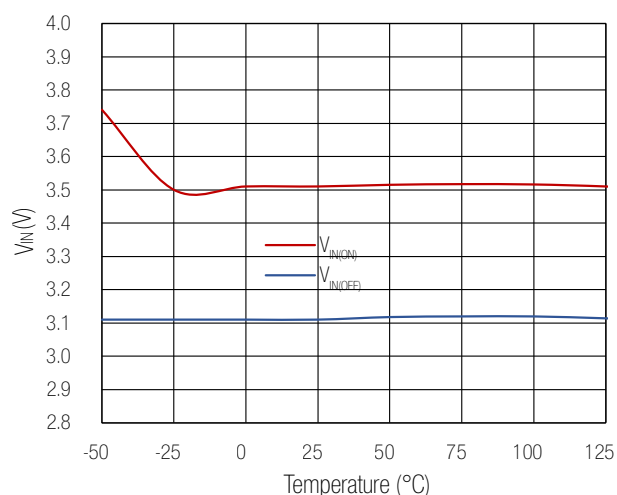


Figure 5. Clamp current vs Drain-source on-voltage drop

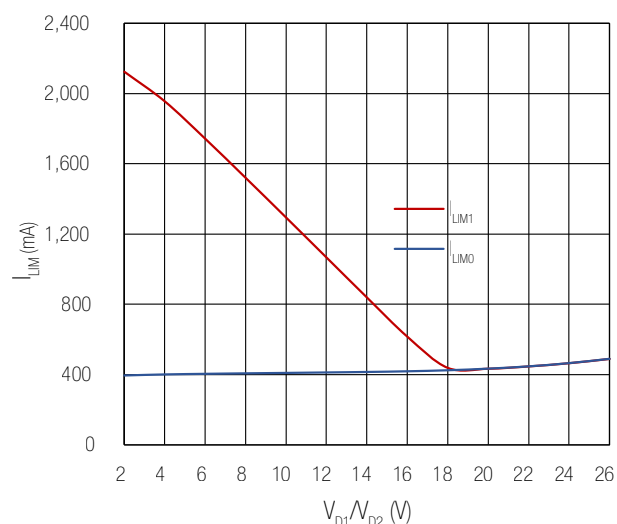
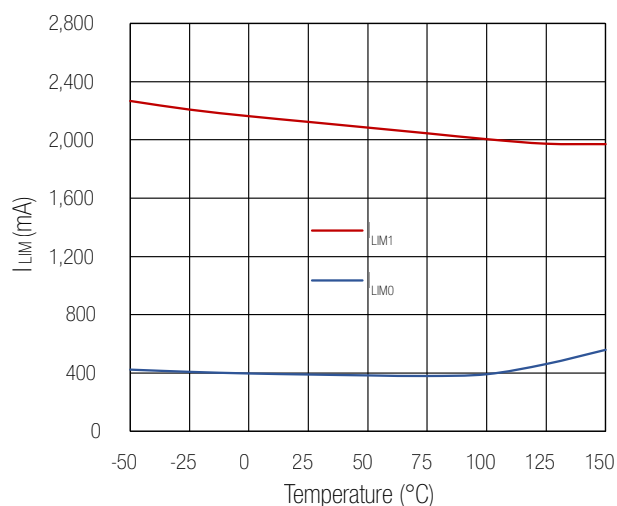


Figure 6. Clamp current vs Temperature

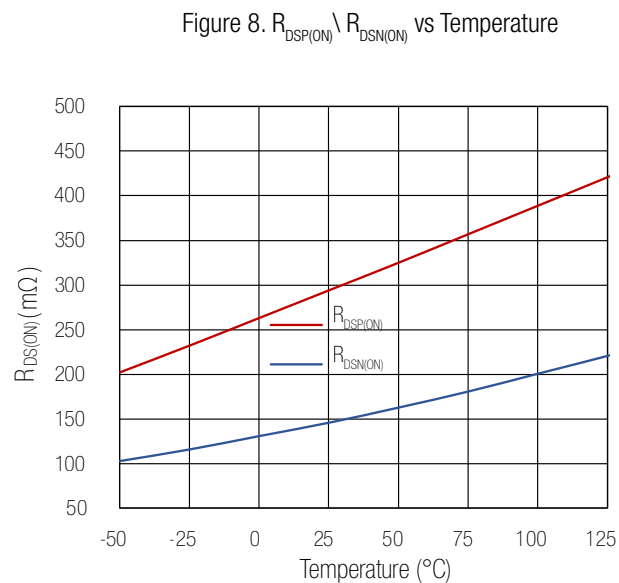
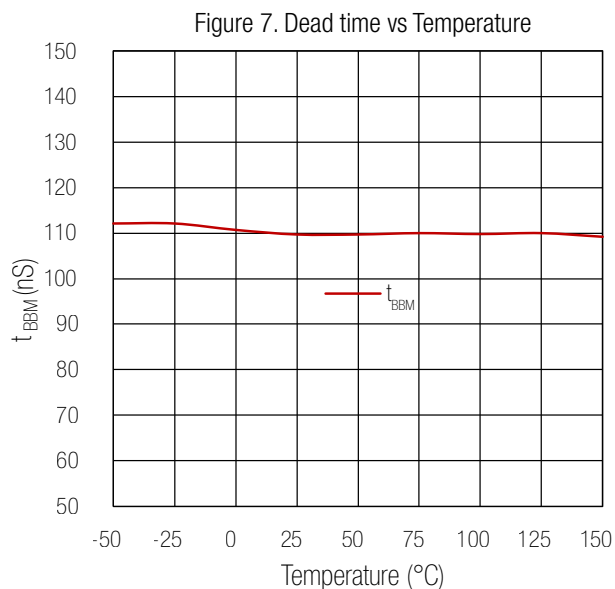


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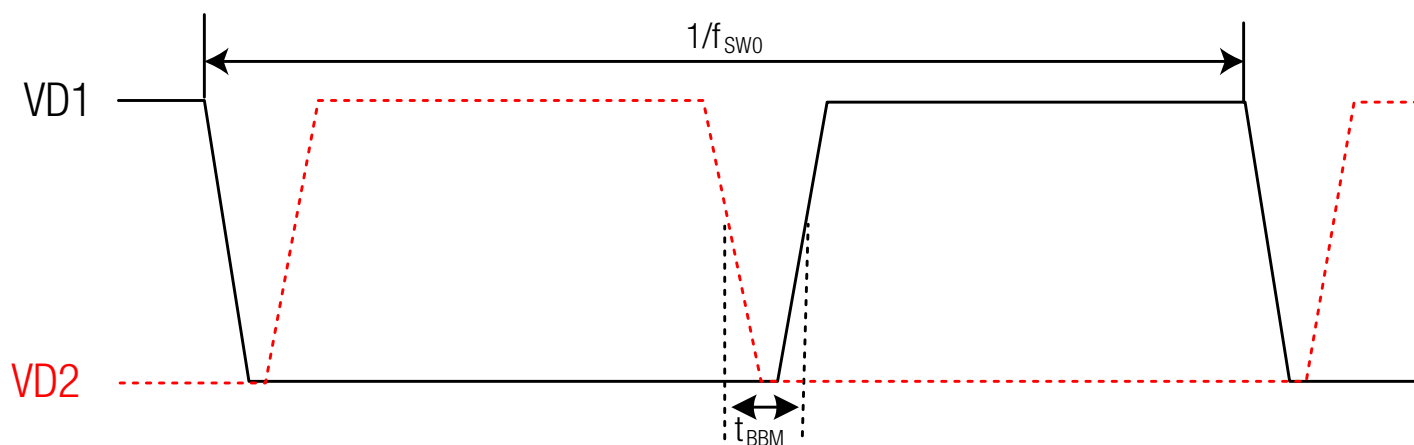
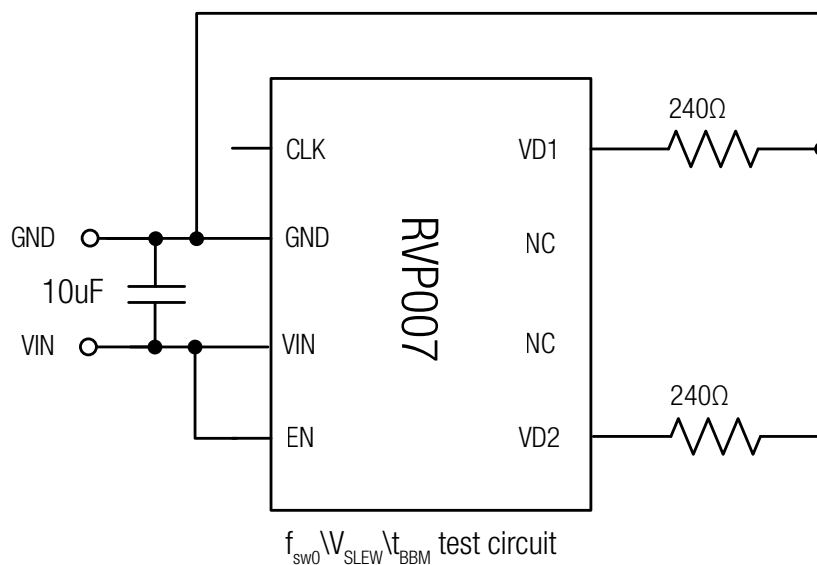
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TECHNICAL SPECIFICATION

Typical characteristic curve

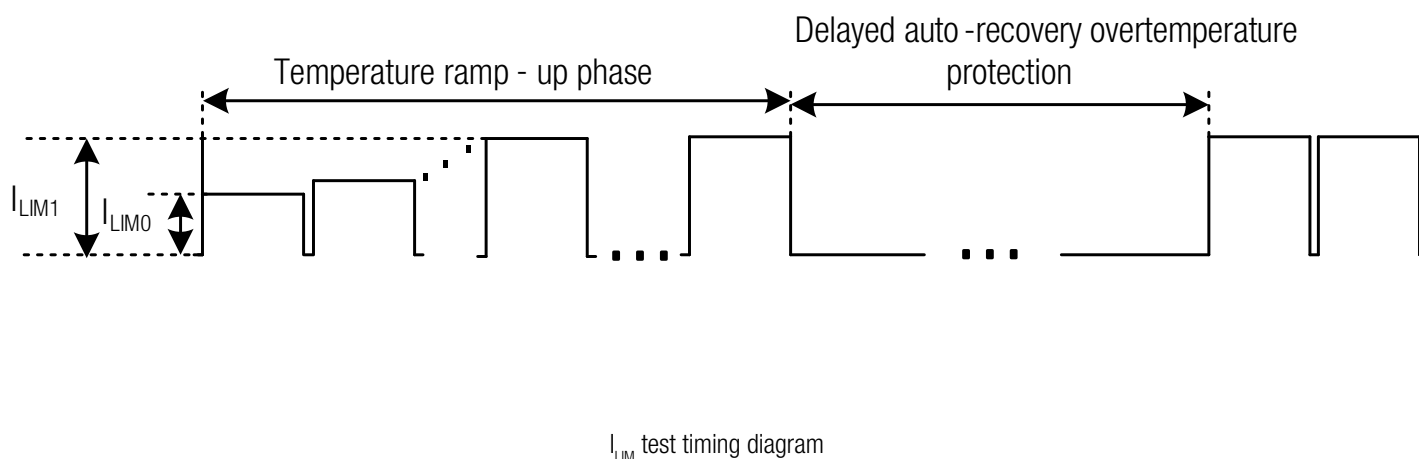
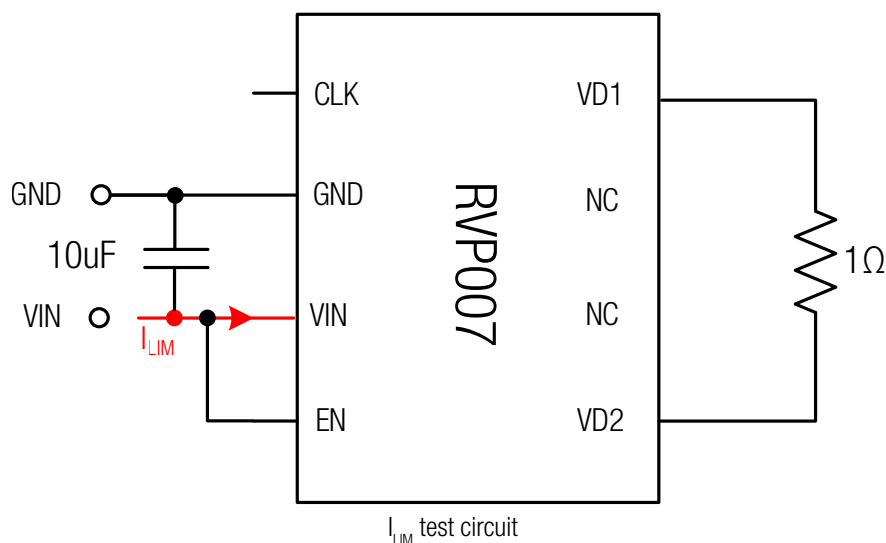


PARAMETER TEST CIRCUIT



VD1 and VD2 pin voltage timing diagram

PARAMETER TEST CIRCUIT



FUNCTIONS AND PRINCIPLES

Overview

The RVP007 is an integrated DC/DC isolated switching power supply controller designed for full-bridge topology applications. The bridge-drive architecture reduces the number of transformer windings and lowers system cost. It supports applications with an input voltage range from 4.5V to 24V, providing strong compatibility across various systems.

When excessive current occurs, the device clamps and limits the power MOSFET current, ensuring that the IC itself operates within a safe operating area while also protecting external components from high-current stress.

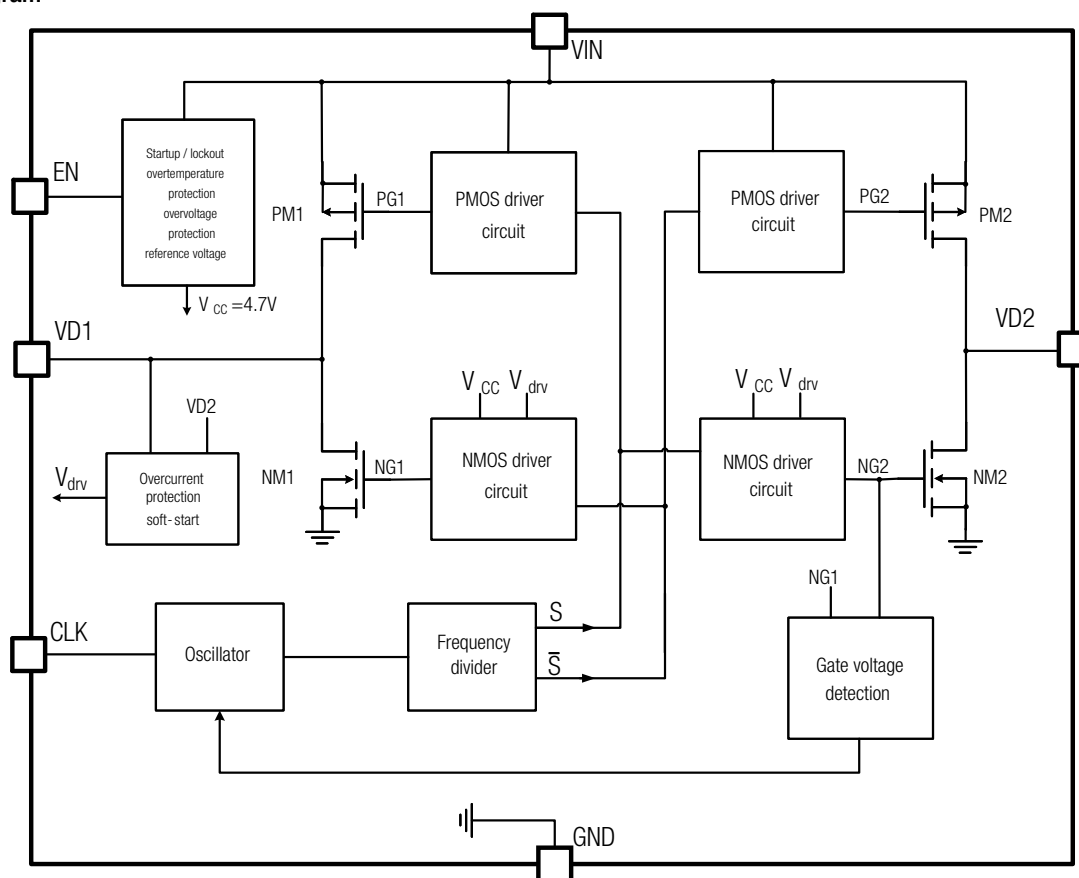
When the CLK pin is left floating, the internal switching frequency f_{SWO} is selected. If a programming resistor from 9 kΩ to 100 kΩ is connected between CLK and GND, the operating frequency is determined by the resistor value.

The EN pin can be used to enable or disable the device. When EN is pulled high (internally pulled high when left floating), the device operates normally. When EN is pulled low, the device stops operating, enabling ultra-low standby power consumption.

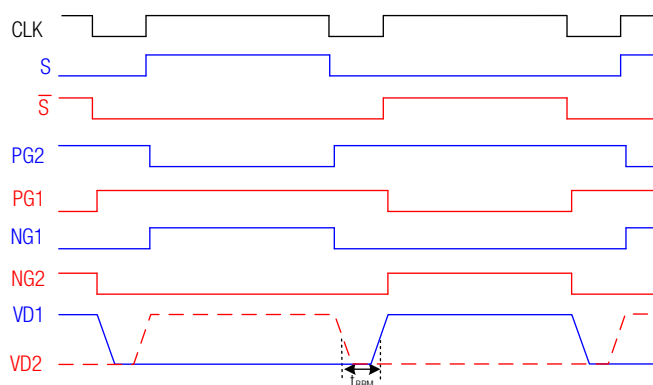
The RVP007 can be used in LLC configuration. For more information about LLC configuration contact techsupport@recom-power.com.

FUNCTIONS AND PRINCIPLES

Functional diagram



Full-bridge drive timing diagram



Drive timing diagram

NG1 and NG2 correspond to the logic levels of the gate voltages of power MOSFETs NM1 and NM2, respectively. They have the same high-level pulse width, with a period during which both signals remain low between the two high-level pulses. This interval is the dead time t_{BBM} , which prevents shoot-through between the two power MOSFETs and enables the MOSFETs to turn on at a lower drain-source voltage, thereby reducing switching losses. When NM1 and NM2 are turned off, their gate voltages are detected. The dead time t_{BBM} is generated only after the MOSFETs are confirmed to be off, preventing driver delay and its temperature coefficient from affecting the dead-time duration, and ensuring consistency across the full input voltage range.

Full-bridge converter

Operating principle of the full-bridge converter

When $S = 0$, the P-channel MOSFET PM1 and the N-channel MOSFET NM2 are turned on, while the P-channel MOSFET PM2 and the N-channel MOSFET NM1 are turned off, forming the first-direction isolated power transfer path:

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FUNCTIONS AND PRINCIPLES

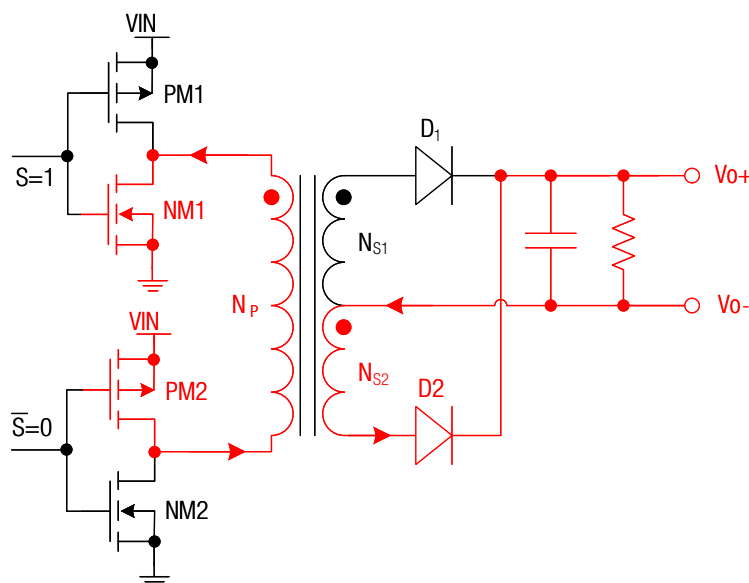
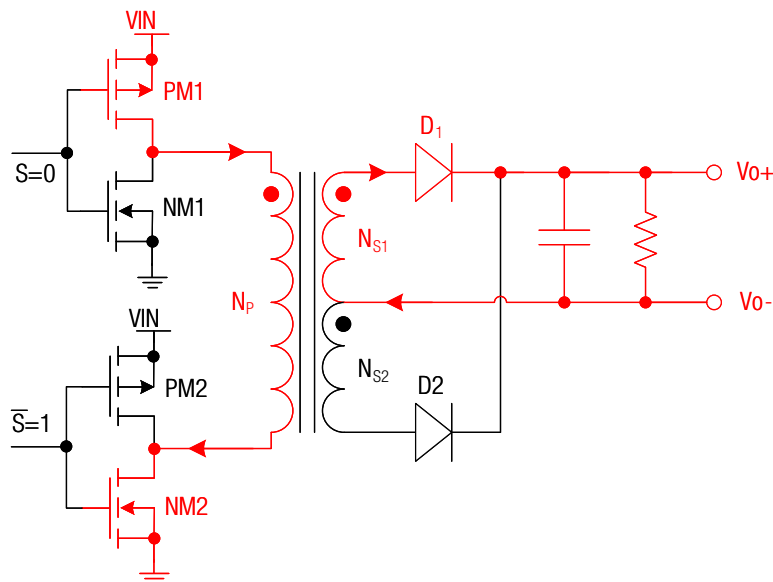
Full-bridge converter

Operating principle of the full-bridge converter

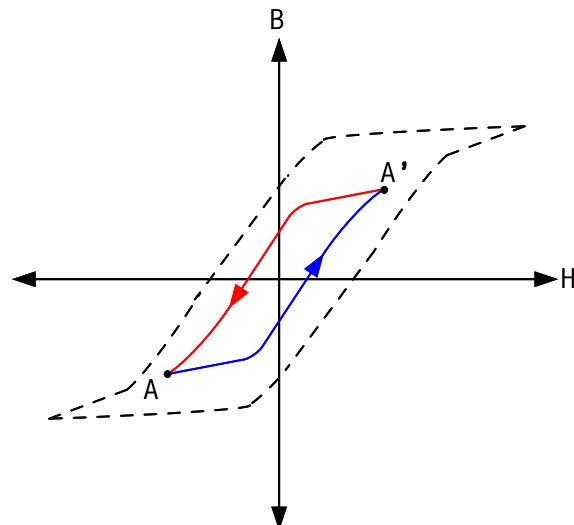
On the transformer primary side, current flows from the positive terminal VIN of the input supply through PM1, enters the dotted terminal of the primary winding NP, exits from the non-dotted terminal, and then flows through NM2 to the input supply ground GND. On the transformer secondary side, current enters the non-dotted terminal of winding NS1 and exits from the dotted terminal. It then passes through the forward-biased rectifier diode D1 to the converter output. During this interval, no current flows through winding NS2, and rectifier diode D2 remains reverse-biased. When $S = 1$, the P-channel MOSFET PM2 and the N-channel MOSFET NM1 are turned on, while the P-channel MOSFET PM1 and the N-channel MOSFET NM2 are turned off, forming the second-direction isolated power transfer path:

On the transformer primary side, current flows from the positive terminal VIN of the input supply through PM2, enters the non-dotted terminal of the primary winding NP, exits from the dotted terminal, and then flows through NM1 to the input supply ground GND. On the transformer secondary side, current enters the dotted terminal of winding NS2 and exits from the non-dotted terminal. It then passes through the forward-biased rectifier diode D2 to the converter output. During this interval, no current flows through winding NS1, and rectifier diode D1 remains reverse-biased. The operating process of the full-bridge converter transfers energy to the secondary side with an effective duty cycle close to 100%, resulting in very high conversion efficiency and excellent dynamic performance. After rectification, only a relatively small output filter capacitor is theoretically required to achieve low output voltage ripple.

However, to prevent shoot-through during the switching transition of the two primary-side switching paths and to minimize switching losses, the controller introduces a certain dead time to ensure reliable operation. During the dead-time interval, the full-bridge transformer cannot transfer energy to the load, and the output capacitor must temporarily supply the load current, which results in a certain amount of output voltage ripple.



Operating principle diagram of the full-bridge converter

FUNCTIONS AND PRINCIPLES**Full-bridge converter****Core magnetization**

Full-bridge transformer core magnetization curve

The normal operation of a full-bridge transformer must satisfy the principle of “volt-second balance,” meaning that the volt-second product generated during the magnetization process of the transformer must equal the volt-second product generated during the demagnetization process. If they are not equal, magnetic core saturation may occur. The core magnetization curve is shown in figure above, where B represents the magnetic flux density of the core and H represents the magnetic field strength inside the core. When switches PM1 and NM2 are turned on, the full-bridge transformer enters the “magnetization” phase, and the magnetic flux density continuously increases along the direction from A to A'. At the moment PM1 and NM2 are turned off, the magnetic flux density reaches its positive maximum value A'. When switches PM2 and NM1 are turned on, the full-bridge transformer enters the “demagnetization” phase, and the magnetic flux density continuously decreases along the direction from A' to A. At the moment PM2 and NM1 are turned off, the magnetic flux density reaches its negative maximum value A. The magnitude of the magnetic flux density B is mainly determined by the product of the primary winding voltage amplitude V_p and the switch conduction time T_{on} during the switching interval, namely $V_p \times T_{on}$, commonly referred to as the “volt-second product.” Proper transformer operation requires compliance with the principle of volt-second balance, meaning that the volt-second product generated during the magnetization process must equal that generated during the demagnetization process. Otherwise, magnetic bias may occur. As the converter continues operating, the accumulation of magnetic bias energy will gradually increase the magnetic flux density in the direction of the bias until it exceeds the saturation flux density range of the magnetic material, ultimately causing core saturation and abnormal operation.

Operating modes**Current clamp drive mode**

During converter startup, output short-circuit conditions, or transformer core saturation, excessive current through the power MOSFETs may be detected. In such cases, the gate drive voltage of power MOSFETs NM1 and NM2 is reduced to limit the current to the current clamp limit value I_{LIM} . This ensures that the MOSFETs operate within their safe operating area while protecting the transformer and output rectifier diodes from excessive current stress, thereby improving converter reliability. In addition, to reduce input inrush current during converter startup, I_{LIM} gradually increases from the initial value I_{LIM0} to I_{LIM1} . To balance capacitive-load driving capability at high input voltage and overload capability at low input voltage, I_{LIM} decreases as the conduction voltage drop across VD1 and VD2 increases.

Delayed auto-recovery overtemperature protection mode

When the internal chip temperature exceeds the specified threshold, the device enters protection mode and disables all power MOSFETs. To resume the power MOSFET drive operation, the following two conditions must both be satisfied: 1. The temperature must fall below the recovery threshold. 2. The forced cooling/rest period must have elapsed. With this protection mechanism, the internal chip temperature after thermal protection recovery is closer to the ambient temperature when restarting. This provides the maximum temperature margin before reaching the thermal shutdown threshold again, allowing a longer MOSFET driving duration. As a result, the device achieves improved capacitive-load driving capability and avoids abnormal startup behavior after thermal protection when operating with large output capacitors.

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FUNCTIONS AND PRINCIPLES

Principle of output short-circuit protection

The output short-circuit protection of the full-bridge converter is achieved through the combined action of the current clamp drive mode and the delayed auto-recovery overtemperature protection mode. When the output is short-circuited, the primary winding NP of the transformer is clamped, resulting in only a small voltage drop across the winding. Most of the input voltage V_{IN} is therefore dropped across the N-channel MOSFETs. As a result, a large current is detected flowing through the power MOSFETs, causing the device to enter current clamp drive mode. Due to the power dissipation of the MOSFETs, the chip temperature gradually rises until the delayed auto-recovery overtemperature protection mode is triggered. Lower ambient temperature or lower input voltage results in a slower temperature rise rate, thereby extending the time required to reach the thermal protection threshold. This mechanism provides adaptive and extremely strong capacitive-load driving capability. Even under high ambient temperature conditions, the delayed recovery mode still optimizes capacitive-load performance.

General operating mode

During the startup phase, the converter output capacitor voltage is low, resulting in relatively large current through the power MOSFETs. Therefore, the converter starts in current clamp drive mode. When the converter output voltage rises close to the rated output voltage, the MOSFET current decreases, and the drive voltage increases to minimize the MOSFET on-resistance.

Enable shutdown mode

When the EN voltage is lower than $V_{EN(OFF)}$, the EN pin outputs an 8μA pull-up current so that the EN pin can be pulled high when left floating. To improve the noise immunity of the EN pin, it is generally recommended to connect EN directly to V_{IN} to provide a stronger pull-up. When the EN voltage exceeds $V_{EN(ON)}$, the internal power supply further enhances the pull-up capability through an additional 80kΩ resistor, enabling normal operation of the RVP007. The temperature characteristics of the turn-on voltage $V_{EN(ON)}$ and turn-off voltage $V_{EN(OFF)}$ are shown in Figure 3.

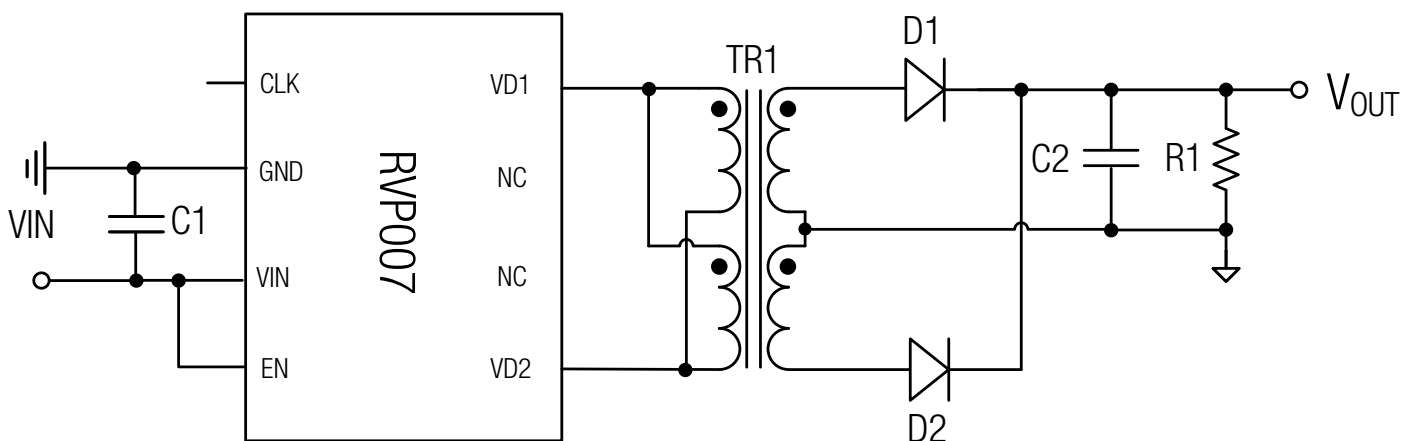
Operating frequency selection

The CLK pin is connected to a unity-gain amplifier with a reference voltage of 1.27V. Connecting a resistor between CLK and GND (or leaving the pin floating) generates different reference currents, which are used to select different operating frequencies. When the CLK pin current is less than 8.5μA, the internal fixed frequency f_{SWO} is selected. When the CLK pin current is greater than 8.5μA, the operating frequency is determined by the frequency programming resistor R_{CLK} . If the internal frequency is selected, it is recommended to leave CLK floating or connect a small filter capacitor of several tens of pF between CLK and GND. If resistor-programmed frequency operation is selected, it is recommended that the programming resistor connected between CLK and GND satisfy $R_{CLK} \leq 100k\Omega$. Under this condition, the approximate operating frequency equation is:

$$f_{SW} = \frac{7500}{R_{CLK}} \quad (\text{kHz})$$

where R_{CLK} is in kΩ.

TYPICAL APPLICATION



Typical application schematic

RVP007 Transformer Driver for Isolated Supplies**4.5-24VIN ◇ 24V ◇ 1.2A Power MOSFET****TYPICAL APPLICATION****Design requirements**

The following typical application example is based on an input voltage of 12 V ±10%, with an isolated non-regulated 5 V output and a maximum output power of 1 W. The related technical specifications of the power supply are as follows:

Input and output specification table

Technical specification	Min.	Typ.	Max.	Unit
Input voltage	10.8	12	13.2	V
Output voltage	-	5	-	V
Output current	-	0.2	-	A
Output ripple + noise	-	50	100	mV
Line regulation	-	-	1.5	%
Load regulation	-	-	10	%
Conversion efficiency	-	85	-	%

Reliability requirements

Output short-circuit protection	Continuous operation with auto-recovery			
Operating temperature	-40	-	85	°C
Isolation voltage	3000	-	-	VDC

Input capacitor selection

As shown in the typical application schematic, the input capacitor C1 serves the functions of energy storage, filtering, and decoupling. The decoupling capacitor should be placed as close to the IC as possible. During operation of the full-bridge converter, capacitor C1 provides transient current to the converter. Therefore, a capacitance value in the range of 1 µF to 10 µF is recommended to reduce input voltage ripple. If necessary, an additional 0.1 µF ceramic decoupling capacitor may be connected in parallel between the VIN and GND pins of the IC. The capacitor voltage rating must satisfy the maximum input voltage requirement while maintaining appropriate derating. It is recommended to use ceramic chip capacitors with low ESR and stable temperature characteristics. Power loop traces should be made as wide and short as possible to minimize unnecessary voltage spikes caused by alternating current flowing through PCB trace inductance during operation.

Output rectifier diode selection

It is recommended to use Schottky diodes with low forward voltage drop and short reverse recovery time for the output rectifier circuit, as this helps achieve better load regulation and higher conversion efficiency for the full-bridge converter. This application uses a full-wave output rectifier structure. The reverse voltage stress on the rectifier diode is twice the output voltage amplitude. Therefore, the reverse voltage rating of the output rectifier diode should be selected to be at least twice the maximum output voltage amplitude under the highest input voltage and minimum load conditions, while ensuring proper derating. The output rectifier diode should be selected to meet the actual operating temperature range requirements. Particular attention should be paid to the fact that the reverse leakage current of a Schottky diode increases significantly at the maximum operating temperature. Therefore, appropriate derating should be applied according to the diode's high-temperature operating characteristics. For details, refer to the temperature derating curve in the diode datasheet.

To ensure reliable and stable operation of the full-bridge converter under all operating conditions, the selection of the output rectifier diode should also consider the maximum operating current under output short-circuit fault conditions. After the RVP007 enters output short-circuit protection mode, the IC automatically switches to current clamp drive mode and limits the MOSFET operating current to the current clamp limit value ILIM. At this time, the maximum operating current of the output rectifier diode can be derived based on the transformer turns ratio and calculated using the following formula:

$$I_{D-MAX} = \frac{N_P}{N_S} \times I_{LIM-MAX}$$

Where NP is the number of turns of the primary winding of the full-bridge transformer, NS is the number of turns of the secondary winding of the full-bridge transformer, and ILIM-MAX is the maximum current clamp limit value of the IC. During operation in output short-circuit protection mode, the full-bridge converter operates in delayed auto-recovery overtemperature protection mode. From the moment the IC enters the auto-recovery operating process until thermal protection is triggered and operation stops, the rectifier diode remains under maximum operating current conditions. Therefore, when selecting the output rectifier diode, it must also be ensured that its forward surge current capability (IFSM – Forward Current Surge Peak) satisfies the application requirements.

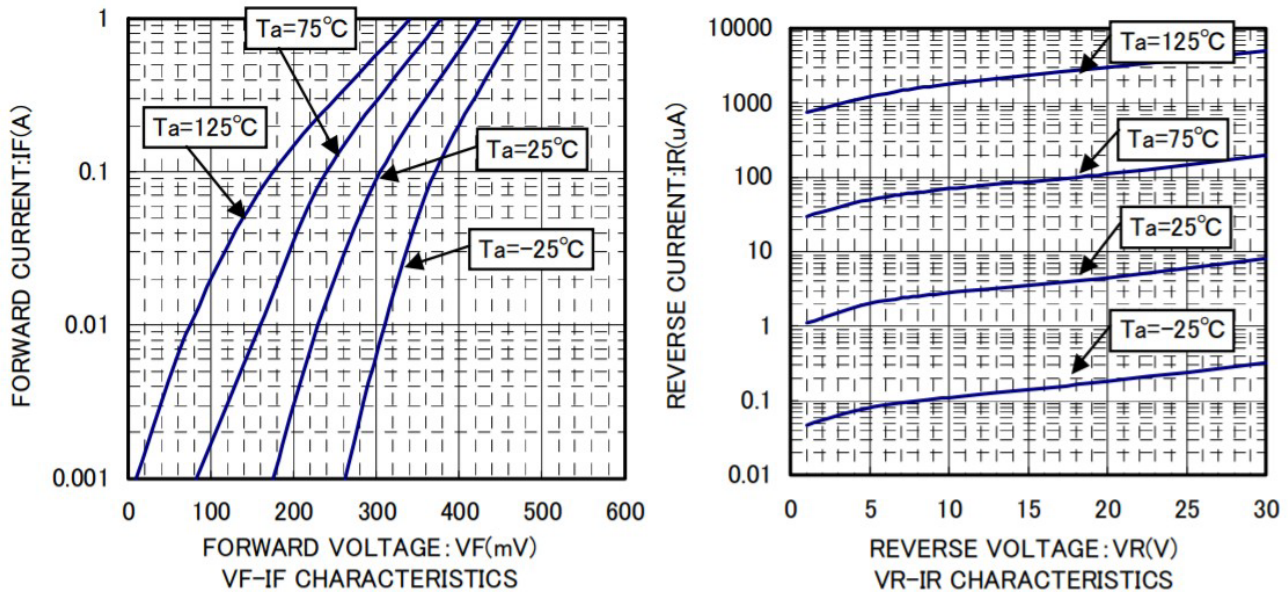
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TYPICAL APPLICATION

Output rectifier diode selection

In this application example, the RB160M-30 Schottky diode may be selected. Under a 75°C operating temperature condition, this diode has a forward voltage drop of approximately 280mV @ 0.2A, a reverse leakage current of approximately 90 μ A @ 15V, and a forward surge current capability of $I_{FSM} = 30$ A. If higher operating temperature requirements are needed, a Schottky diode with lower reverse leakage current at elevated temperatures should be selected.



RB160M-30 Schottky diode operating characteristic curves

Output capacitor selection

The full-bridge converter can theoretically transfer energy to the secondary side with a 100% duty cycle. However, to ensure reliable operation of the converter, a certain dead time must be reserved during the switching transition between the two bridge legs to prevent shoot-through. During the dead time, the output energy is mainly supplied by the output filter capacitor C3, resulting in a certain amount of output ripple. In practical applications, a 4.7 μ F to 10 μ F ceramic capacitor is recommended for C3 to achieve better filtering performance for the converter.

Full-bridge transformer selection

Estimation of the primary-to-secondary winding turns ratio

Assuming the output rectifier diode of the full-bridge converter has been selected according to the design requirements, the forward voltage drop VF of the rectifier diode under maximum output load conditions can be obtained. The primary-to-secondary winding turns ratio of the full-bridge transformer can then be estimated based on the input voltage across the primary winding and the minimum output voltage on the secondary winding.

Under nominal input and full-load output conditions, the input voltage across the primary winding of the full-bridge transformer is:

$$V_P = V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} (R_{DSP(ON)} + R_{DSN(ON)})$$

Where P_{O-MAX} is the maximum output power of the full-bridge converter, η is the estimated conversion efficiency of the full-bridge converter under nominal input and full-load conditions, and $R_{DSP(ON)}$ and $R_{DSN(ON)}$ are the on-resistances of the IC's integrated P-MOSFET and N-MOSFET, respectively.

Under full-load output conditions, the minimum output voltage of the secondary winding is:

$$V_S = V_{O-MIN} + V_F$$

Where V_{O-MIN} is the minimum allowable output voltage of the full-bridge converter under full-load conditions. To ensure that the output voltage characteristic curve meets the specification requirements over the full load range, V_{O-MIN} can be estimated as 97% of the nominal output voltage, corresponding to -3% accuracy from the nominal output voltage. VF is the forward voltage drop of the selected output rectifier diode under full-load conditions.

TYPICAL APPLICATION**Full-bridge transformer selection****Estimation of the primary-to-secondary winding turns ratio**

Based on the above equations, the calculation formula for the primary-to-secondary winding turns ratio can be obtained as follows:

$$N_{PS} = \frac{V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} \times (R_{DSP(ON)} + R_{DSN(ON)})}{V_{O-MIN} + V_F}$$

Based on the input and output requirements of this application example, the primary-to-secondary winding turns ratio of the full-bridge transformer can be estimated as:

$$N_{PS} = \frac{12V - \frac{1W}{0.85 \times 12V} \times (0.60\Omega + 0.25\Omega)}{5V \times 0.97 + 0.34V} \approx 2.3$$

Full-bridge transformer volt-second product estimation

To prevent transformer saturation, the volt-second product of the selected full-bridge transformer must be greater than the maximum volt-second product generated by the RVP007 under all normal operating conditions. In narrow-input-range isolated power supply applications, the input range is typically specified as $\pm 10\%$ of the nominal input voltage. Therefore, the volt-second product of the full-bridge transformer should be calculated based on the upper limit of the power supply input voltage. In addition, the IC's programmed frequency and tolerance should also be considered to ensure that saturation does not occur under the minimum operating frequency condition. The maximum volt-second product applied by the RVP007 to the transformer primary winding occurs at the highest input voltage and during half of the switching period corresponding to the programmed minimum operating frequency. Therefore, the minimum volt-second product of the full-bridge transformer can be estimated using the following calculation method:

$$Vt_{MIN} \geq V_{IN-MAX} \times \frac{T_{MAX}}{2} = \frac{V_{IN-MAX}}{2 \times f_{MIN}}$$

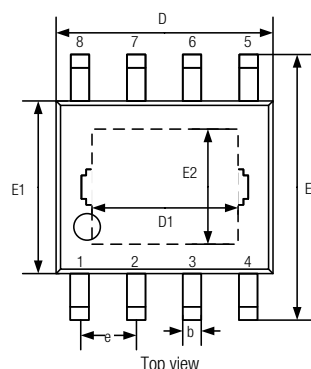
Based on the design requirements of this application example, assuming the programmed typical operating frequency is 250 kHz and the minimum operating frequency is 220 kHz, under the maximum input voltage condition, the selected full-bridge transformer shall satisfy the following volt-second product requirement:

$$Vt_{MIN} \geq \frac{12V \times 110\%}{2 \times 220KHz} \approx 30V\mu s$$

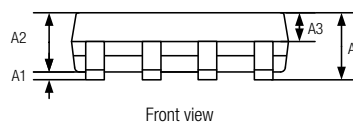
The full-bridge transformer should be selected according to the actual application requirements, with appropriate volt-second product and primary-to-secondary winding turns ratio. In addition, the maximum output power, isolation voltage rating, and isolation parasitic capacitance should also be considered as important reference factors when selecting the full-bridge transformer.

RVP007 Transformer Driver for Isolated Supplies

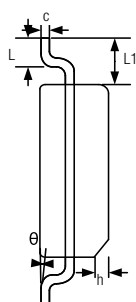
4.5-24VIN ◇ 24V ◇ 1.2A Power MOSFET

PACKAGING INFORMATION**ESOP8**

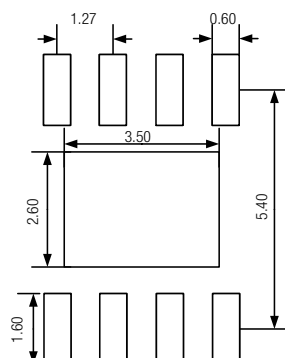
Top view



Front view



Side view



Recommended pad

Dimension table

Symbol	Millimeter		
	Min.	Nom.	Max.
A	-	-	1.65
A1	0	-	0.15
A2	1.3	1.4	1.5
A3	0.6	0.65	0.7
b	0.39	-	0.47
c	0.2	-	0.24
D	4.8	4.9	5
D1	3.1 REF		
E	5.8	6	6.2
E1	3.8	3.9	4
E2	2.21 REF		
e	1.27 BSC		
h	0.25	-	0.5
L	0.5	0.6	0.8
θ	0°	-	8°

ORDER INFORMATION

Part number	Package	PIN	Package type	SPQ	Marking code*	MSL
RVP007-FBN-R	ESOP8	8	Tape and reel	4000	RVP007	MSL-3
RVP007-FBN-CT	ESOP8	8	Moisture barrier bag	10	RVP007	MSL-3

*Marking code

RVP007 — Product code

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