RVP005 Transformer Driver for Micro-power Isolated Supplies

6-30VIN/30V/0.6A Power Switch

FEATURES

- Full Bridge Topology
- Open Loop LLC Drive Mode Available
- Highly Integrated, Simple Solution
- Built-in 30V/0.25Ω NMOS
- Built-in 30V/0.60Ω PMOS
- 0.9A Current Clamp Limit
- 6-30V Input Voltage Range
- Surge Voltage up to 38V
- Internal or External Clock Source
- Adaptive Dead Time Control
- Enable Control Pin
- Built-in Soft Start
- Output Short-circuit Protection, Over-temperature Protection, Self-recovery
- Ambient: -40°C to +125°C

APPLICATIONS

- IGBT/SiC Gate-drive Power Supplies
- Isolated Interface Auxiliary Power Supplies
- Precision and Medical Equipment
- DCS/PLC Auxiliary Power Supplies
- UPS and PV Inverter Systems
- Distributed/Radio/Telecom Power Supplies

DESCRIPTION

RVP005 is a transformer driver specifically designed for compact, micro-power isolated power supplies with ultra-low standby power consumption. It requires only minimal external components-input/output filter capacitors, an isolation transformer, and a rectifier circuit-to build an efficient isolated power supply with a 6-30V input voltage range, multiple output voltage options, and output power from 1W to 10W.

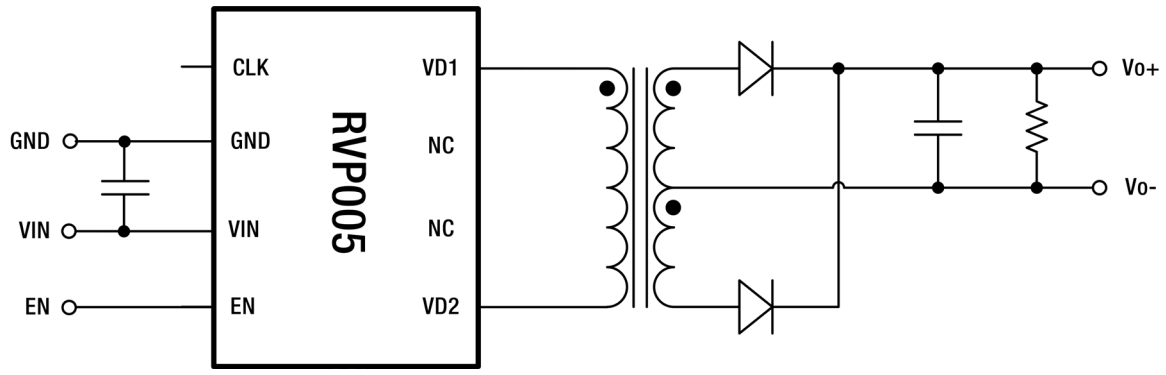
RVP005 integrates two N-channel and two P-channel power switches configured in a full-bridge topology. It features an internal oscillator that generates a pair of high-precision complementary signals, ensuring symmetrical switching to prevent magnetic core bias during operation.

The device supports both internal and external clock sources, offering flexible timing control. When using an external clock via the CLK input, the RVP005 outputs a pair of complementary signals at half the input clock frequency. Its integrated dead-time control circuitry ensures precise timing and safe operation under various conditions. Comprehensive protection features are built-in, including overcurrent protection, overtemperature protection, and self-recovery mechanisms to safeguard the device from damage under fault conditions such as output short circuits.

Device information

Part Number	Package	Weight(mg)	Dimension	SPQ
RVP005	ESOP8	77.00	5.0mm x 6.0mm	4000

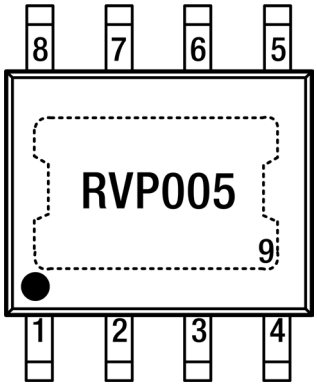
SIMPLIFIED SCHEMATIC



RVP005 Transformer Driver for Micro-power Isolated Supplies

6-30VIN/30V/0.6A Power Switch

PIN CONFIGURATION AND FUNCTIONS



Name	No.	Type	Description
CLK	1	I	The external clock input pin (CLK) is used to configure the clock source and the dead time adaptation function. When the CLK pin is held high-either driven high or left floating (due to the internal pull-up)-the internal clock frequency is automatically set to 250kHz, and the dead time t_{BBM} remains fixed. When the CLK pin is connected to GND, the internal clock frequency remains at 250kHz, but the dead time t_{BBM} operates in adaptive mode. If an external clock signal is applied to the CLK pin, enabling the clock synchronization function allows symmetric complementary drive signals to be generated after passing through a frequency divider.
GND	2	P	Logic circuit ground and analog circuit ground.
VIN	3	P	Power input, VIN to GND with a 1uF capacitor; place the capacitor as close to the device as possible.
EN	4	I	Enable pin. The transformer stops operating when the pin voltage is at low potential and operates normally when it is not connected or at high level.
VD2	5	O	Transformer drive output 2.
NC	6, 7	-	No functional pin
VD1	8	O	Transformer drive output 1.
EP	9	P	Exposed Pad should be connected to GND to enhance heat dissipation. The use of multi-layer PCBs with thermal vias is recommended to improve heat transfer. Bare pads should not be used as electrical connection points.

SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
VIN Input Voltage	V_{IN}	-0.3	38	V
LDMOS drain voltage	VD1, VD2	-0.3	V_{IN} +0.3	V
LDMOS peak current	$I_{(VD1)PK}$, $I_{(VD2)PK}$		1.6	A
EN/CLK Pin Voltage	EN, CLK	-0.3	6.6	V
Peak Junction Temperature	T_{JMAX}		150	°C
Storage Temperature Range	T_{STG}	-55	150	°C

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model HBM, per ESDA/JEDEC JS-001-2017; (Zap 1 pulse, Interval :>=0.1S)	±2000	V
		Charged device model CDM, per ESDA/JEDEC JS-002-2014	±1000	V

(1)JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Resistance

Packaging	θ_{JA}	Ψ_{JT}	UNIT
ESOP8	51.9	6.5	°C/W

Note: Measured on a test board with 1oz copper (7.62cm × 11.43cm).

Recommended Operatings Conditions

		MIN	TYP	MAX	UNIT
VIN Input Voltage	V_{IN}	6		30	V
Output switch current-Primary side	I_{VD1}, I_{VD2}			0.6	A
Ambient Temperature	T_A	-40		125	°C

Electrical Characteristics

VIN= 12V, T= 25°C, unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Supplies						
V_{IN}	Input voltage range		6		30	V
$V_{IN(ON)}$	Switch-on voltage	EN unconnected, V_{IN} rising	4.3	4.8	6	V
$V_{IN(HYS)}$	Hysteresis voltage	EN unconnected, V_{IN} falling		0.3		V
IQ	V_{IN} quiescent current	VD1, VD2, CLK, EN unconnected	1.5	2.1	2.8	mA
$I_{VIN(EN)}$	V_{IN} current after EN disabled	EN=0		19	30	uA
Enable Pin EN						
$V_{EN(ON)}$	EN turn-on voltage	V_{EN} rising		2.1	2.5	V
$V_{EN(HYS)}$	EN shutdown hysteresis	VEN falling	0.7	1.0	1.3	V
$I_{EN(SRC)}$	Current source of EN	V_{EN} rises to $V_{EN(ON)}$ +0.1V		13	40	uA
Output Interface VD1/ VD2						
DMM	VD1/VD2			0%		
$R_{DSN(ON)}$	NMOSFET on resistance	T=25°C, I_{DS} =0.2A		0.25		Ω
		T=100°C, I_{DS} =0.2A		0.34		
$R_{DSP(ON)}$	PMOSFET on resistance	T=25°C, I_{DS} =0.2A		0.60		
		T=100°C, I_{DS} =0.2A		0.80		
V_{SLEW}	Voltage slew rates	240Ω resistor between VD1 and VD2		350		V/us
t_{BBM}	break-before-make time	240Ω resistor between VD1 and VD2, CLK unconnected		180		ns
$t_{BBM(MAX)}$	Maximum Break-before-make time	10kΩ resistor between VD1 and VD2, CLK connects to GND		500		ns
I_{LIM0}	Current clamp limit initial value	Short circuit VD1 and VD2, test current of I_{VIN}. VIN=6V	0.40	0.52	0.70	A
I_{LIM1}	Current clamp limits steady-state values		0.65	0.9	1.30	A
t_{SS}	Soft-start time			1		mS
Frequency pin CLK						
F_{SW0}	Average switching Frequency	CLK unconnected	225	250	275	kHz
$V_{CLK(H)}$	CLK High level logic voltage			2.2	2.5	V
$V_{CLK(L)}$	CLK low level logic voltage		0.7	1.2		V
$F_{(EXT)}$	External clock frequency on CLK pin		50		1600	kHz
Over Temperature Protection						
T_{SHDN}	Thermal shutdown		145	162	178	℃
$T_{SHDN(HYS)}$	Thermal shutdown hysteresis			27		℃
$T_{OFFMIN(OTP)}$	Minimum shutdown time			2^{18}		Tsw

Typical Characteristics

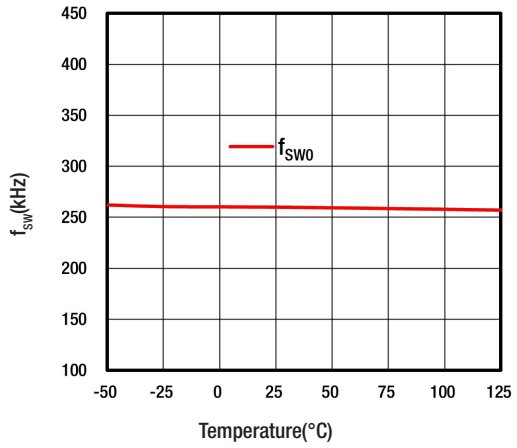


Fig. 1 Frequency vs Temperature

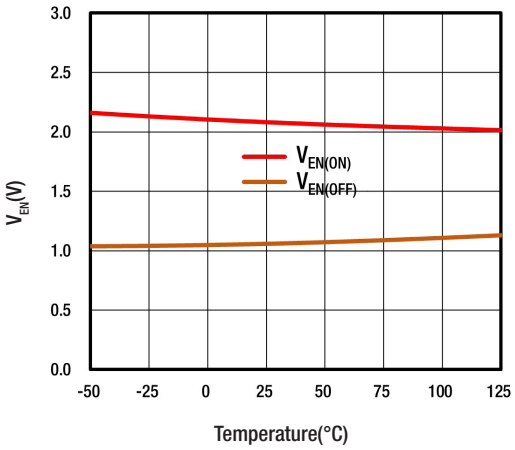


Fig. 2 V_{EN} vs Temperature

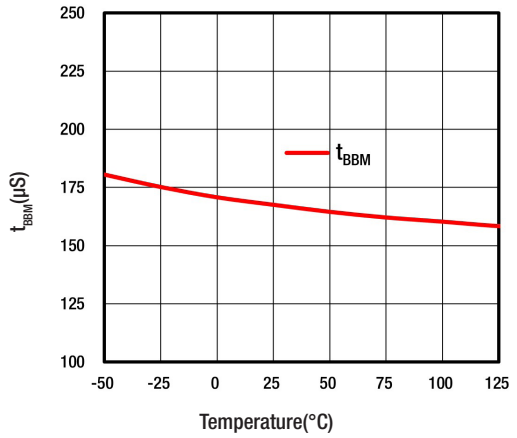


Fig. 3 t_{BBM} vs Temperature

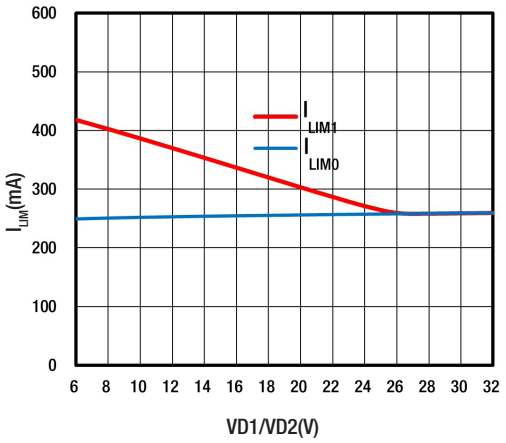


Fig. 4 I_{LIM} vs Drain conduction voltage drop

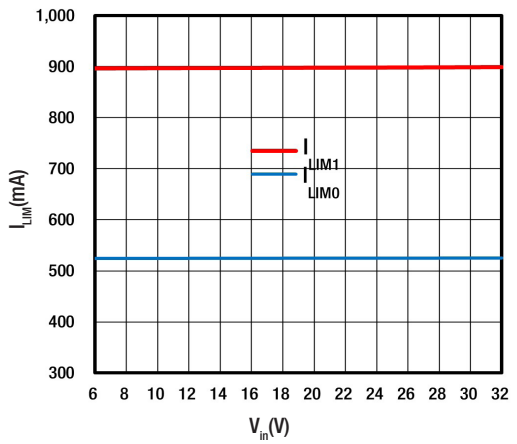


Fig. 5 I_{LIM} vs Input Voltage

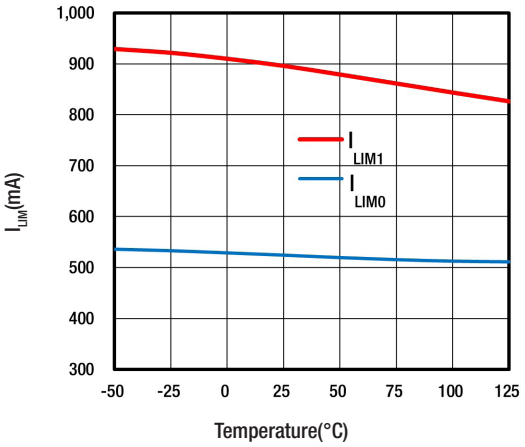


Fig. 6 I_{LIM} vs Temperature

PARAMETER MEASUREMENT INFORMATION

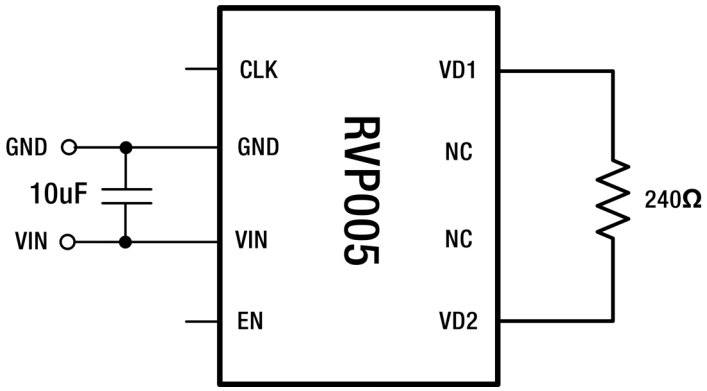


Fig. 7 f_{sw0}/ V_{SLEW}/ t_{BBM} Test Circuit

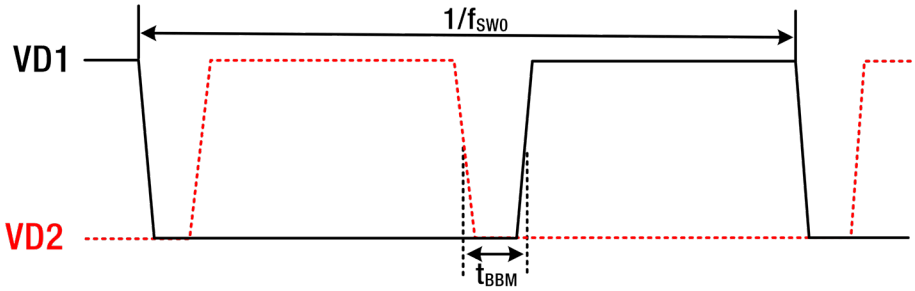


Fig. 8 VD1 and VD2 Timing Diagram

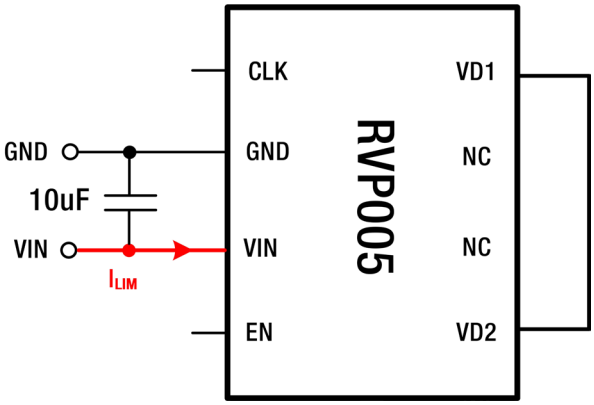


Fig. 9 I_{LIM} Test Circuit

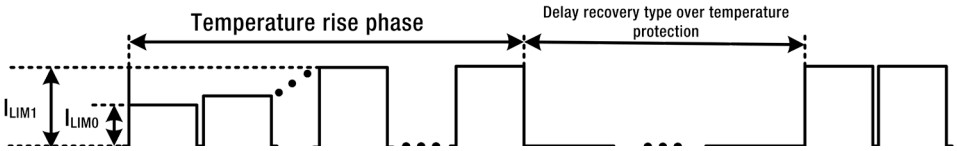


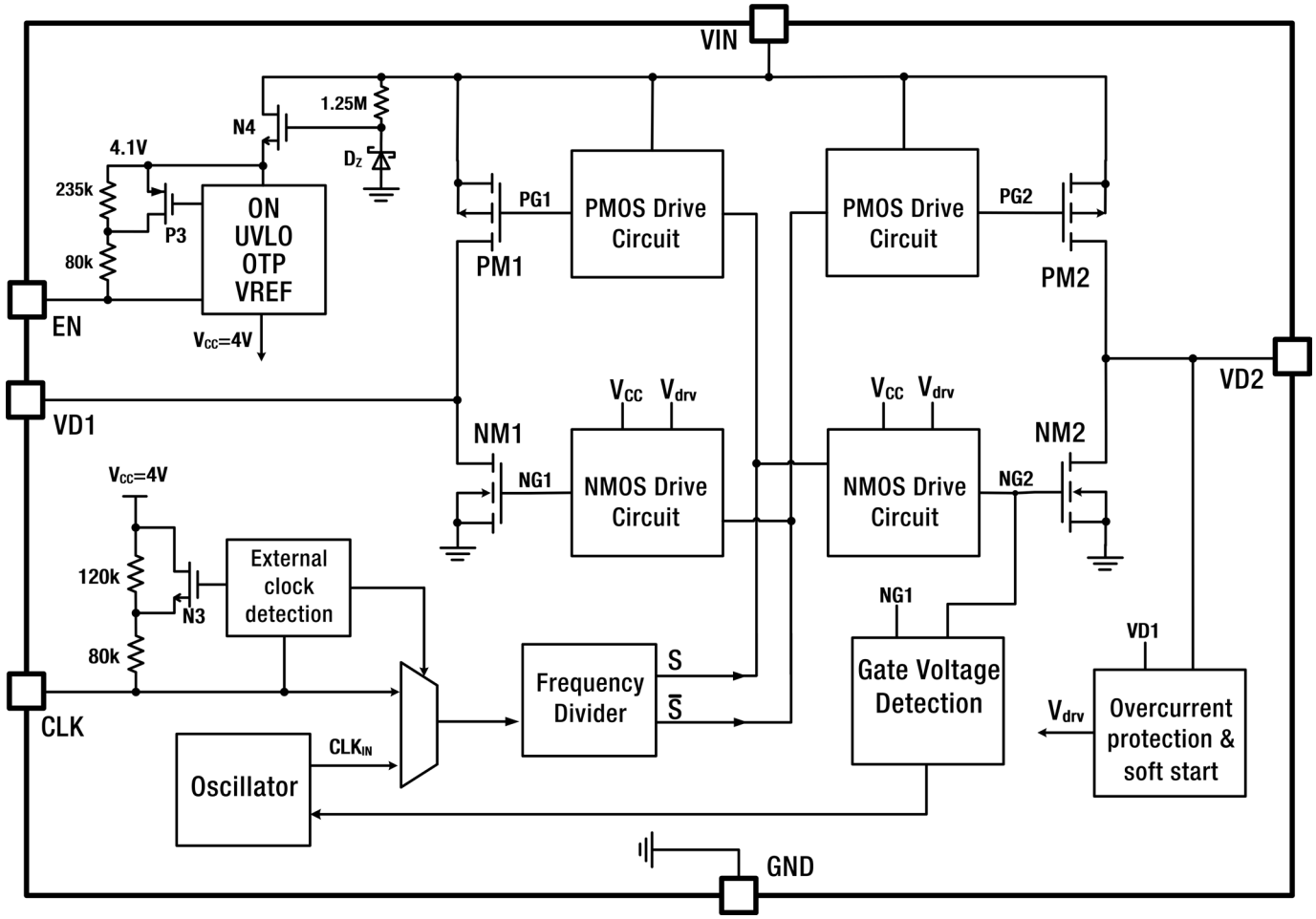
Fig. 10 I_{LIM} Test Timing Diagram

DETAILED DESCRIPTION

Overview

RVP005 is a transformer driver designed for isolated DC/DC converters utilizing a full bridge topology. This topology effectively reduces the number of transformer windings, contributing to lower overall cost. The device supports a wide input voltage range of 6V~30V, offering strong compatibility with various applications. It features a clamping mechanism that limits power switch current when it becomes excessively high, ensuring the chip operates within a safe zone while also protecting surrounding components from potential damage caused by large current surges. When CLK pin is left floating (internally pulled up to a high level) or connected to ground, internal switching frequency (f_{SW0}) is automatically selected. In this configuration, dead time remains fixed when the CLK pin is floating, but becomes adaptive when the CLK pin is grounded. Power switches activate after the drain voltage drops, enabling zero-voltage switching to enhance efficiency and reduce electromagnetic interference (EMI). CLK pin also supports external synchronization, with the output frequency set to half of the input clock frequency. The chip is controlled via the EN pin. When EN is pulled high or left unconnected, in which case it is automatically pulled high the chip operates normally. When EN is pulled low, device stops operating and enters an ultra-low standby power consumption mode.

FULL FUNTIONAL BLOCK DIAGRAM



OPERATION MODE

Full Bridge Waveform

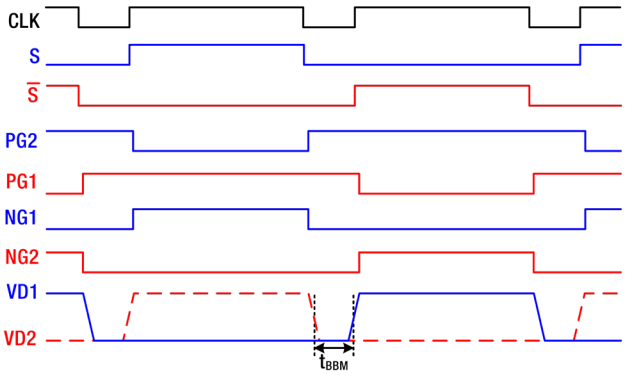


Fig. 11 Output Signal Waveforms

In Figure 11, NG1 and NG2 correspond to the logic levels of the gate voltages for power switches NM1 and NM2, respectively. Both signals have identical high-level pulse widths, with a brief interval between their high states during which all signals remain low. This interval is known as the dead time, t_{BBM}, which is implemented to prevent shoot-through and to allow the power switches to turn on at a lower drain-source voltage, thereby reducing switching losses. The dead time t_{BBM} is primarily determined by the low-level period of the oscillator clock (CLK), and its duration is inversely related to the operating frequency of the chip-the lower the frequency, the longer the dead time, and vice versa. When NM1 and NM2 are turned off, the gate voltage is monitored, and t_{BBM} is generated only after the power switches are fully turned off. This approach helps eliminate the effects of driver delay and its temperature dependence, ensuring consistent dead time performance across the full input voltage range.

Current Clamp Mode

During converter start-up, if the output is short-circuited or the transformer becomes magnetically saturated, the current through the power switches is detected to be excessively high. In response, the gate drive voltage of power switches NM1 and NM2 is reduced to limit the current according to the current clamp threshold I_{LIM}. This mechanism not only ensures that the power switches operate within safe limits, but also protects the transformer and output rectifier diode from damage caused by high current, thereby enhancing the overall reliability of the converter.

Delay Recovery Overtemperature Protection Mode

When the internal temperature of the chip exceeds a predefined threshold, the device enters a protection state in which all power switches are disabled. To return to normal operation, two conditions must be met: 1. the temperature must fall below the recovery threshold, and 2. a mandatory cooldown period must be completed. In this protection mode, when the chip restarts after an overtemperature event, its internal temperature is closer to the ambient temperature. As the temperature rises again toward the overtemperature threshold, the chip experiences a larger temperature difference range. This allows for a longer maximum drive time of the power switches, providing greater capacitive load capability and preventing abnormal startup behavior under conditions of high output capacitance.

Principle of Output Short Circuit Protection

The output short-circuit protection of the full bridge converter is achieved through the combined action of current clamp mode and delayed recovery over-temperature protection. When an output short circuit occurs, the voltage drop across the transformer's primary winding N_P is minimal, causing most of the input voltage VIN to drop across the N-channel MOSFETs. Upon detection of a large current, the chip enters current clamp mode. As the power switches continue to conduct under high current, the chip temperature gradually increases, eventually triggering the over-temperature protection with a built-in delay before recovery. Rate of temperature rise and thus the time taken to activate thermal protection is influenced by ambient temperature and input voltage: lower ambient temperatures or lower VIN values result in slower temperature rise, allowing longer operation before protection is triggered. This behavior enables adaptive, robust support for capacitive loads. Even in high-temperature environments, the delayed recovery mechanism enhances performance under heavy capacitive loading conditions.

General Operating Mode

During start-up, the output capacitor voltage is initially low, causing a relatively high current through the power switches. As a result, the converter starts in current clamp mode to limit excessive current. As the output voltage approaches the rated value, the current through the power switches decreases. At this stage, the gate drive voltage increases, reducing the ON-resistance of the switches and improving overall efficiency.

EN Shutdown Mode

The Zener diode DZ, NMOS transistor N4, and a 1.25MΩ bias resistor form a 4.1V voltage source that provides the bias voltage for the enable (EN) pin. Inside the device, the pull-up resistance at the EN pin consists of two resistors 235kΩ and 80kΩ connected in series. When the EN voltage exceeds the enable threshold voltage $V_{EN(ON)}$, the RVP005 begins normal operation, and PMOS transistor P3 turns on. In this state, the effective pull-up resistance at the EN pin is 80 kΩ, which enhances noise immunity. Conversely, when the EN voltage drops below the disable threshold $V_{EN(OFF)}$, the chip disables output, PMOS P3 turns off, and the effective pull-up resistance at the EN pin becomes 315kΩ, helping to reduce standby power consumption. The temperature characteristics of the enable and disable threshold voltages $V_{EN(ON)}$ and $V_{EN(OFF)}$ are shown in Functional Block Diagram.

Operating Frequency Selection

CLK pin supports clock synchronization. When an external clock signal is applied to the CLK pin, the signal is processed through a frequency divider to generate complementary driver signals. In this mode, the RVP005 operates at half the frequency of the external clock. The device also includes an internal clock. If the CLK pin remains continuously high or low for six internal clock cycles CLK_{IN}, the RVP005 automatically switches to using the internal clock as its operating frequency. When the CLK pin is connected to ground GND, the dead time enters adaptive operation mode. In this mode, the power switches are turned on only after a drop in the drain voltage VD1/VD2 is detected, enabling zero-voltage switching ZVS. If the voltage drop is not detected within the maximum allowed wait time $t_{BBM(MAX)}$, the power switches will be turned on regardless, ensuring continuous operation.

Full Bridge Converter

Operating principle of full bridge converter

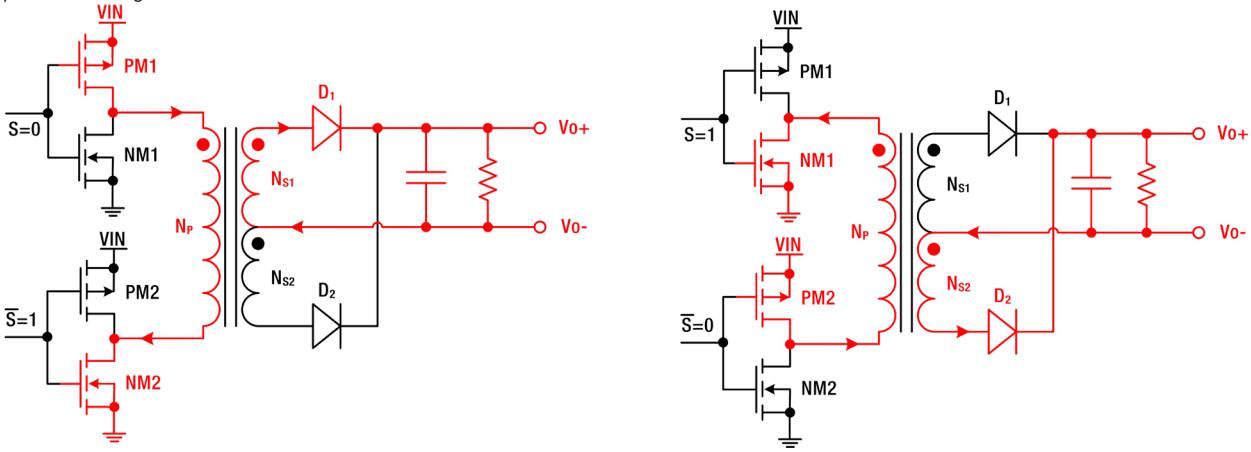


Fig. 12 Full Bridge Transformer Schematic

When S = 0, the P-channel MOSFET PM1 and N-channel MOSFET NM2 are turned on, while PM2 and NM1 are turned off, establishing the first direction of isolated energy transmission. On the primary side of the transformer, current flows from the input voltage source VIN through PM1, enters the dotted terminal of the primary winding N_P, exits from the non-dotted terminal, flows through NM2, and returns to ground. On the secondary side, current flows through winding NS1 and then passes through the rectifier diode D_1 to reach the converter's output. During this state, no current flows through winding NS2, and diode D_2 remains off.

When S = 1, PM2 and NM1 are turned on, while PM1 and NM2 are turned off, establishing the second direction of isolated transmission. Current flows from VIN through PM2 into the transformer's primary winding N_P, and returns to ground through NM1. On the secondary side, current flows through winding NS2 and then through the conducting rectifier diode D_2 to the output terminal. In this state, winding NS1 carries no current, and diode D_1 remains off.

The full bridge converter operates at nearly a 100% duty cycle, which allows continuous energy transfer to the secondary side, resulting in high conversion efficiency and excellent dynamic response. After rectification, only a relatively small output capacitor is needed to maintain a low ripple voltage. However, to avoid shoot-through conditions between the switching MOSFETs on the primary side and to minimize switching losses, a certain dead time is introduced by the controller. During this brief dead time, the full bridge transformer is unable to transfer energy to the load, and the output capacitor temporarily supplies power, resulting in a small increase in output voltage ripple.

Core Magnetization

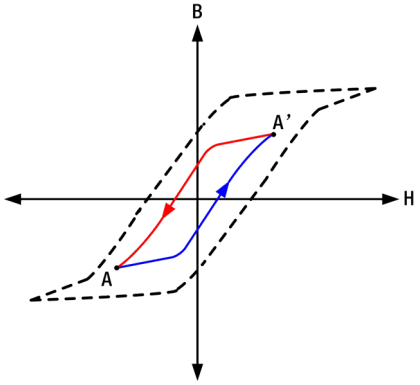


Fig. 13 Full Bridge Transformer Core Magnetization

For a full bridge transformer to operate normally, it must satisfy the condition known as volt-second balance. This principle states that the volt-second product the product of the primary winding voltage (V_P) and the duration of conduction time (T_{ON}) during the magnetization excitation phase must be equal in magnitude and opposite in polarity to that of the demagnetization phase. If this balance is not maintained, core saturation may occur over time.

Figure 13 illustrates the magnetization curve of a transformer core, where B denotes magnetic flux density and H represents magnetic field strength within the core.

When switches PM1 and NM2 are turned on, the transformer enters the excitation phase, and magnetic flux density increases as the flux moves from point A to A'. This causes the core to store magnetic energy, and when these switches are turned off, the flux reaches its maximum positive value at point A'.

Subsequently, when switches PM2 and NM1 are turned on, the transformer enters the demagnetization phase, during which the magnetic flux density decreases as the flux returns from A' to A. When these switches are turned off, the core reaches its maximum negative magnetic flux density at point A.

The magnitude of the magnetic flux density B in each cycle is primarily governed by the volt-second product, expressed as $V_P \times T_{ON}$. For balanced operation, the volt-second product in the excitation phase must match that of the demagnetization phase. If an imbalance occurs, it introduces a magnetic bias-a gradual shift in the core's operating point along the B-H curve. Over time, this bias accumulates and pushes the core toward magnetic saturation, exceeding its designed flux density limit. Once saturation is reached, the core can no longer support proper energy transfer, resulting in loss of transformer function and potential failure of the converter.

TYPICAL APPLICATION (EP IS CONNECTED TO GND BY DEFAULT)

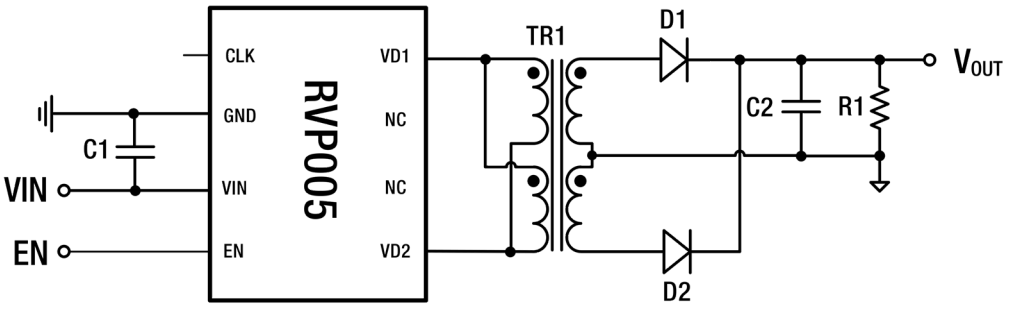


Fig. 14 Typical Application Schematic

Design Requirements

The following are some typical applications with an input voltage of 12V±10%, an isolated unregulated 5V output, and a maximum output power of 1W. Technical specifications of the power supply are shown below:

Input and Output Parameters

Specification	MIN	TYP	MAX	UNIT
Input Voltage	10.8	12.0	13.2	V
Output Voltage	---	5.0	---	V
Output Current	---	0.2	---	A
Output Ripple and Noise	---	50	100	mV
Voltage Regulation	---	---	1.5	%
Load Regulation	---	---	10	%
Conversion Efficiency	---	85	---	%
Reliability Requirements				
Output Short Circuit Protection		Continuous, self-recovery		
Operating Temperature	-40	---	85	°C
Isolation	3000	---	---	VDC

Input Capacitor Selection

As shown in Figure 14, the input capacitor C1 serves multiple purposes, including energy storage, input filtering, and decoupling. Enhancing high-frequency noise suppression, an additional 0.1μF ceramic capacitor may be connected in parallel between VIN and GND. This decoupling capacitor should be placed as close to the chip as possible.

During operation, C1 supplies transient current to the converter. A capacitance value in the range of 1μF to 10μF is recommended to minimize input voltage ripple. The capacitor's voltage rating must exceed the maximum input voltage, with appropriate derating applied.

For optimal performance, use ceramic chip capacitors with low ESR and stable temperature characteristics. To further reduce voltage spikes caused by parasitic PCB inductance, place C1 close to the VIN and GND pins, and ensure that power loop traces are short and wide.

Output Rectifier Diode Selection

For optimal performance, it is recommended to use Schottky diodes in the output rectification circuit due to their low forward voltage drop and short reverse recovery time, which contribute to improved load regulation and higher conversion efficiency. This design adopts a full-wave rectification topology, where the reverse voltage stress on each diode is approximately twice the output voltage. Therefore, the selected diode must have a reverse voltage rating of at least 2x the maximum output voltage, with appropriate derating applied for reliability.

The selected rectifier diode must also be capable of operating reliably across the expected ambient temperature range. Special attention should be given to reverse leakage current, which increases significantly at high temperatures. Derating based on the diode's temperature-leakage characteristics (as illustrated in the diode's temperature derating curve) is necessary to maintain performance and reliability.

To ensure the full-bridge converter operates reliably under all conditions, the diode selection must also account for abnormal operating scenarios, such as output short circuits. In such cases, the RVP005 enters output short-circuit protection mode, during which it switches to current clamp mode. The internal clamp limits the current through the power switches to I_{LIM} (typically 0.9A, up to 1.3A maximum). As a result, the maximum current through the output rectifier diode must be calculated based on the transformer turns ratio and this clamped primary current.

The peak current requirement for the rectifier diode can be estimated using the following formula:

$$I_{D-MAX} = \frac{N_P}{N_S} \times I_{\mathrm{LIM-MAX}}$$

In the equation, N_P refers to the number of turns of the primary winding of the full-bridge transformer, N_S is the number of turns of the secondary winding, and $I_{LIM-MAX}$ represents the maximum current clamp limit of the chip.

During protection mode, the converter operates in over-temperature protection (OTP) with delayed recovery. When the chip enters self-recovery and subsequently re-triggers OTP, it shuts down again to prevent thermal damage. During this interval, the output rectifier diode conducts continuously at its maximum operating current. Therefore, when selecting the rectifier diode, it is highly important to ensure that its peak forward surge current (I_{FSM}) rating is sufficient to handle this stress reliably.

The RB160M-30 Schottky diode is suitable for this application. At 75°C, it exhibits a forward voltage drop of approximately 280mV at 0.2A, and a reverse leakage current of around 90μA at 15V. Its peak forward surge current rating is I_{FSM}=30A. For applications requiring higher operating temperatures, it is advisable to select a Schottky diode with lower reverse leakage current under elevated thermal conditions to maintain efficiency and reliability.

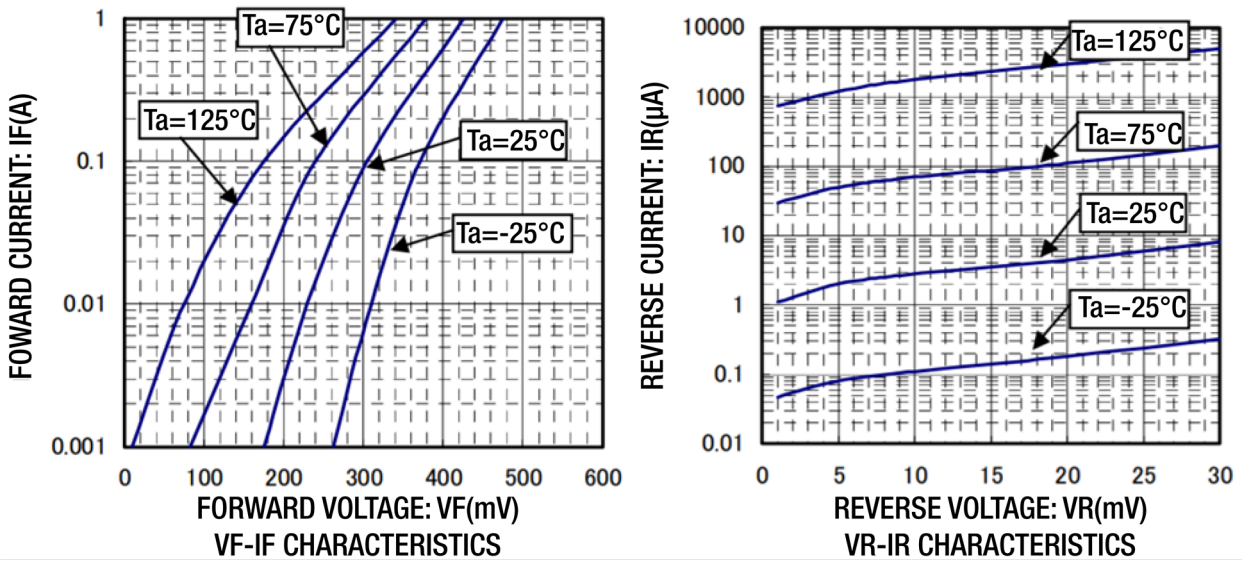


Fig. 15 Schottky Diode RB160M-30 Characteristics

Output Capacitor Selection

While a full bridge converter can theoretically deliver power to the secondary side with nearly a 100% duty cycle, in practice, a short dead time is required between switching transitions to prevent cross conduction. During this dead time, the output filter capacitor C2 temporarily supplies energy to the load, resulting in some level of output voltage ripple.

To ensure stable operation and effective filtering, it is recommended to use a ceramic capacitor with a capacitance value between 4.7µF and 10µF for C2. The capacitor should have low ESR and good temperature stability to minimize ripple and maintain performance across varying load and environmental conditions.

Full Bridge Transformer Selection

Primary to Secondary turns ratio estimation once the output rectifier diode has been selected, its forward voltage drop (V_F) at maximum output current can be determined. This value, along with the target output voltage, helps define the required minimum secondary voltage. The turns ratio of the full bridge transformer primary winding (N_P) to secondary winding (N_S) can then be estimated based on the input voltage on the primary side and the minimum required output voltage on the secondary side. Using this information, the transformer can be designed to ensure that the required output voltage is delivered while maintaining efficient power transfer, proper volt-second balance, and sufficient headroom for rectification losses and regulation margin.

Under nominal input and full-load conditions, the input voltage across the transformer's primary winding is:

$$V_p = V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} (R_{DSP(ON)} + R_{DSN(ON)})$$

P_{O-MAX} is the maximum output power of the full bridge converter, η is the nominal input, estimated conversion efficiency of a full bridge converter at full load, and $R_{DSP(ON)}$ and $R_{DSN(ON)}$ are ON-resistance of the PMOS and NMOS respectively.

At full output load, the minimum output voltage of the secondary winding is:

$$V_S = V_{O-MIN} + V_F$$

V_{O-MIN} is the minimum output voltage allowed by the full-bridge converter under full-load conditions. To ensure the output remains within specification, V_{O-MIN} is typically calculated as 97% of the nominal output voltage, reflecting a -3% regulation margin. VF represents the forward voltage drop of the selected output rectifier diode at full load.

According to the above equation, the primary to secondary turns ratio can be determined through:

$$N_{PS} = \frac{V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} \times (R_{DSP(ON)+}R_{DSN(ON)})}{V_{O-MIN+}V_F}$$

Based on the input and output requirements of this application, the primary and secondary turns ratio is approximated as:

$$N_{PS} = \frac{12V - \frac{1W}{0.85 \times 12V} \times (0.60\Omega + 0.25\Omega)}{5V \times 0.97 + 0.34V} \approx 2.3$$

Volt-second Product Calculation

To prevent transformer saturation, the volt-second product of the transformer must be greater than the maximum volt-second product generated by the RVP005 under all normal operating conditions. For applications where the isolated power supply has a narrow input range, ±10% of the nominal input voltage is commonly specified as the input range of the power supply and therefore the volt-second product should be calculated based on the upper limit of the power supply input voltage. The frequency and tolerance of the chip should also be considered so that saturation will not occur when the minimum operating frequency is met. The maximum volt-second product applied to the primary winding of the transformer is generated when the minimum operating frequency corresponds to half of the switching cycle with the highest input voltage. As a result, the minimum volt-second product can be calculated as:

$$Vt_{MIN} \geq V_{IN-MAX} \times \frac{T_{MAX}}{2} = \frac{V_{IN-MAX}}{2 \times f_{MIN}}$$

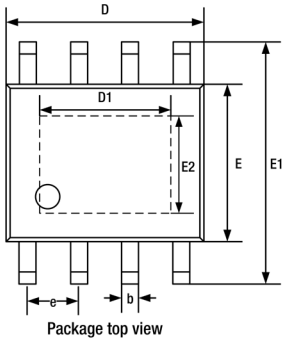
Based on the design requirements of this application, the operating frequency of RVP005 is typically 250kHz and the minimum operating frequency is 228kHz. When the input voltage is at the highest, the volt-second product should be:

$$Vt_{MIN} \geq \frac{12V \times 110\%}{2 \times 228KHz} \approx 28.95V\mu s$$

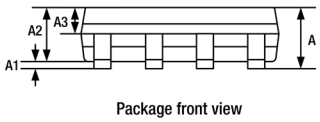
The full bridge transformer selection should be based on the actual application requirements for the appropriate volt-second product and turns ratio. Furthermore, the maximum output power, isolation voltage ratings and distributed isolation capacitance are also important factors to consider when looking

PACKAGING INFORMATION

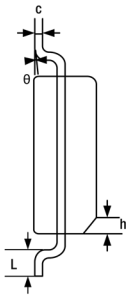
ESOP8



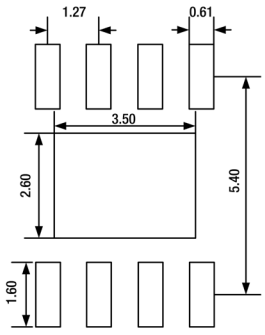
Package top view



Package front view



Package side view



Recommended solder pads

DIMENSION TABLE			
SYMBOL	MILLIMETER		
	MINIMUM	NOMINAL	MAXIMUM
A	1.50	1.60	1.70
A1	0.04	---	0.12
A2	1.35	1.45	1.55
A3	0.65	0.70	0.75
b	0.35	---	0.50
c	0.19	---	0.25
D	4.80	4.90	5.00
D1	3.20	3.30	3.40
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
E2	2.30	2.40	2.50
e		1.27BSC	
h	0.30	---	0.50
L	0.50	---	0.80
θ	0°	---	8°

ORDER INFORMATION

Device	Package Type	PIN	Packaging Method	QTY	Marking Code*	MSL
RVP005-FBN-R	ESOP8	8	Tape and Reel	4000	RVP005	MSL-3

*Marking Code :
RVP005—— Product Code