RVP003S Transformer Driver for Micro-power Isolated Supplies

6-30VIN/30V/0.3A Power Switch

FEATURES

- Full Bridge Topology
- Highly Integrated, Minimal External Components Required
- Integrated 30V / 0.25Ω N-channel MOSFETs
- Integrated 30V / 0.60Ω P-channel MOSFETs
- 0.45A Current Limiting Clamp
- Wide Input Voltage Range: 6V to 30V
- Surges Voltage up to 38V
- Optional Internal Clock or External Frequency Synchronization
- Enable Pin for Power-Down Control
- Integrated Soft-start Function
- Built-in Protection: Continuous Short-circuit, Overtemperature, and Automatic Recovery
- Ambient: -40°C~+125°C

APPLICATIONS

- Low-power Isolated Power Supplies for CAN/RS-485/RS-232/SPI/I2C
- Industrial Process Control Systems
- Precision Instrumentation and Medical Devices
- Distributed/Radio/Telecom Power Supplies
- Low Noise Isolated Power Supplies for USB Applications
- Low Noise Power Supplies for Filament Circuits
- Isolated Power Supplies for IGBT Gate Drivers

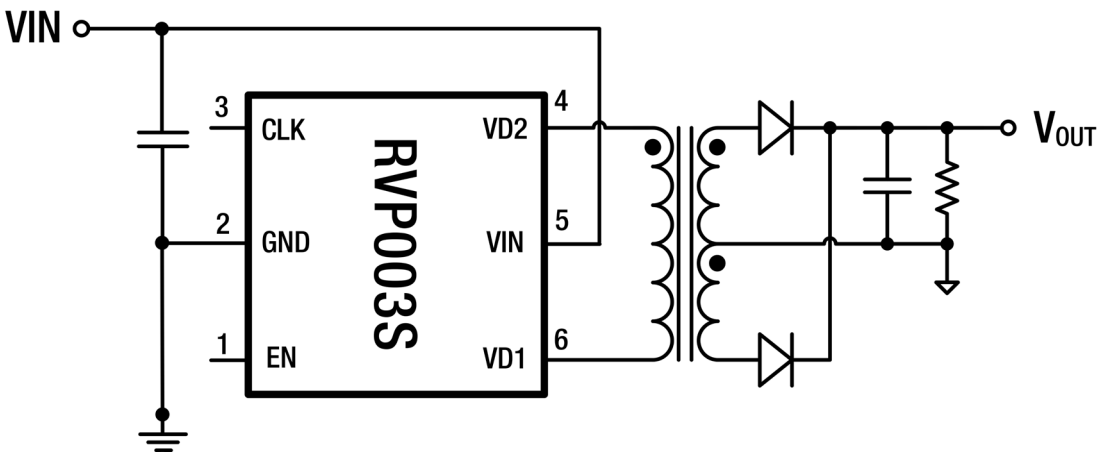
DESCRIPTION

The RVP003S is a transformer driver optimized for compact, low-power isolated power supplies with minimal standby power consumption. It requires only basic external components input/output filter capacitors, an isolation transformer, and rectifier circuits to build an isolated power supply with an input voltage range of 6 to 30V, multiple output voltage options, and output power up to 2W. RVP003S integrates two N-channel and two P-channel MOSFETs configured in a full bridge topology. An internal oscillator generates a pair of high-precision complementary signals, ensuring symmetrical switching to prevent magnetic core bias during operation.The device also features frequency synchronization and multiple protection mechanisms. The RVP003S integrates frequency synchronization capability along with multiple protection features. When an external clock signal is applied to the CLK input, the device outputs two complementary drive signals at half the frequency of the input clock. An internal high-precision dead time control circuit ensures reliable operation by preventing simultaneous conduction of the full-bridge power switches under all operating conditions.

Device information

Part Number	Packaging	Weight(mg)	Size	SPQ
RVP003S	SOT23-6	14.59	3.0mm x 2.8mm	3000

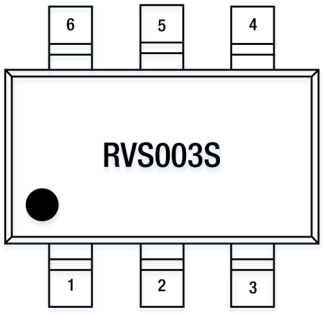
SIMPLIFIED SCHEMATIC



RVP003S Transformer Driver for Micro-power Isolated Supplies

6-30VIN/30V/0.3A Power Switch

PIN CONFIGURATION AND FUNCTIONS



Name	SOT23-6	Type	Description
CLK	3	I	Internal Clock Selection and External Clock Input Pin: This pin allows the selection between internal and external clock sources. When left floating, the internal oscillator operates at a typical frequency of 250kHz. Connecting the pin to GND increases the frequency to 350kHz. If an external clock signal is applied, the device generates symmetrical complementary drive signals through an internal frequency divider.
GND	2	P	Logic circuit ground and analog circuit ground.
EN	1	I	Enable Pin: The chip is disabled when the pin is low; it operates normally when left unconnected or driven high.
VD1	6	O	Transformer drive output 1.
VIN	5	P	Power Input (VIN): Connect a 1µF capacitor between VIN and GND. For optimal performance, position the capacitor as close to the device as possible.
VD2	4	O	Transformer drive output 2.

SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
VIN Input Voltage	V_{IN}	-0.3	38	V
LDMOS Drain Voltage	VD1, VD2	-0.3	V_{IN} +0.3	
LDMOS Peak Current	$I_{(VD1)PK}$, $I_{(VD2)PK}$		1.2	A
EN/CLK	EN, CLK	-0.3	6.6	V
Peak Junction Temperature	T_{JMAX}		150	°C
Storage Temperature Range	T_{STG}	-55	150	°C

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human body model HBM, per ESDA/JEDEC JS-001-2017; (Zap 1 pulse, Interval :>=0.1S)	±2000	V
		Charged device model CDM, per ESDA/JEDEC JS-002-2014	±1000	V

Thermal Resistance

Packaging	θ_{JA}	Ψ_{JT}	UNIT
SOT23-6	143	17.37	°C/W

Note: Measured on a test board with 1oz copper (7.62cm × 11.43cm).

Recommended Operatings Conditions

		MIN	TYP	MAX	UNIT
VIN Input Voltage	V_{IN}	6		30	V
Output Switch Current	I_{VD1} , I_{VD2}			0.3	A
Ambient Temperature	T_A	-40		125	°C

Electrical Characteristics

V_{IN}= 12V, T= 25°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Pin VIN						
V_{IN}	Input voltage range		6		30	V
$V_{IN(ON)}$	Start up voltage	EN unconnected, V_{IN} rising	4.3	4.8	6	V
$V_{IN(HYS)}$	Hysteresis voltage	EN unconnected, V_{IN} falling		0.3		V
IQ	VIN quiescent current	VD1, VD2, CLK, EN unconnected	1.5	2.1	2.8	mA
$I_{VIN(EN)}$	VIN current after EN disabled	EN=0		19	30	uA
Enable Pin EN						
$V_{EN(ON)}$	EN pin logic high threshold	V_{EN} rising		2.1	2.5	V
$V_{EN(HYS)}$	EN pin logic low threshold	V_{EN} falling	0.7	1.0	1.3	V
$I_{EN(SRC)}$	Current source of EN	V_{EN} rises to $V_{EN(ON)}$ +0.1V		13	40	uA
Output Interface VD1/ VD2						
DMM	VD1/VD2			0%		
$R_{DSN(ON)}$	NMOSFET-on resistance	T=25°C, I_{DS} =0.2A		0.25		Ω
		T=100°C, I_{DS} =0.2A		0.34		
$R_{DSP(ON)}$	PMOSFET-on resistance	T=25°C, I_{DS} =0.2A		0.60		
		T=100°C, I_{DS} =0.2A		0.80		
V_{SLEW}	Slew rate	240Ω resistor between VD1 and VD2		350		V/us
t_{BBM}	VD1/VD2 break-before-make time	240Ω resistor between VD1 and VD2		180		ns
I_{LIM0}	Current clamp limit initial value	Short-circuit VD1 and VD2, with VIN=6V. Test the current value of I_{VIN}	180	250	350	mA
I_{LIM1}	Current clamp limits steady-state values		350	450	600	mA
t_{SS}	Rise time when I_{LIM0} rises to I_{LIM1}			1		mS
Frequency pin CLK						
F_{SW0}	Built-in low frequency	CLK unconnected	225	250	275	KHz
F_{SW1}	Built-in high frequency	CLK connects to GND	315	350	385	KHz
$V_{CLK(H)}$	CLK High level logic voltage			2.2	2.5	V
$V_{CLK(L)}$	CLK low level logic voltage		0.7	1.2		V
$F_{(EXT)}$	External synchronous clock		50		1600	KHz

Typical Characteristics

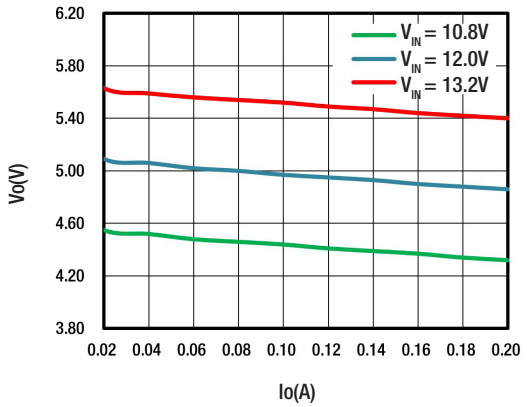


Fig. 1 Output Voltage vs Output Current
(12V to 5V/1W)

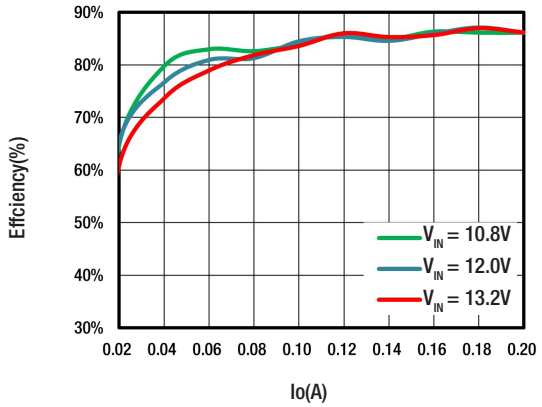


Fig. 2 Conversion Efficiency vs Output Current
(12V to 5V/1W)

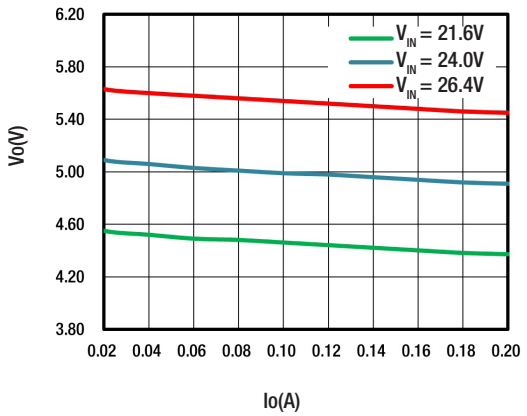


Fig. 3 Output Voltage vs Output Current
(24V to 5V/1W)

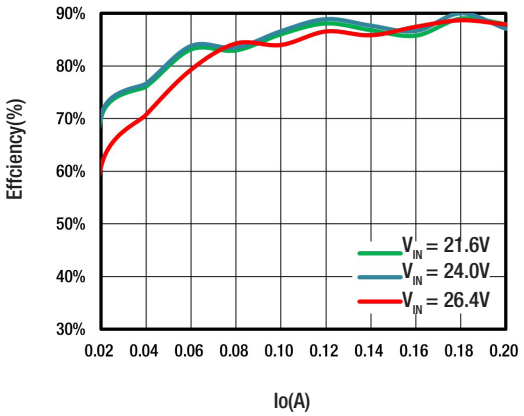


Fig. 4 Conversion Efficiency vs Output Current
(24V to 5V/1W)

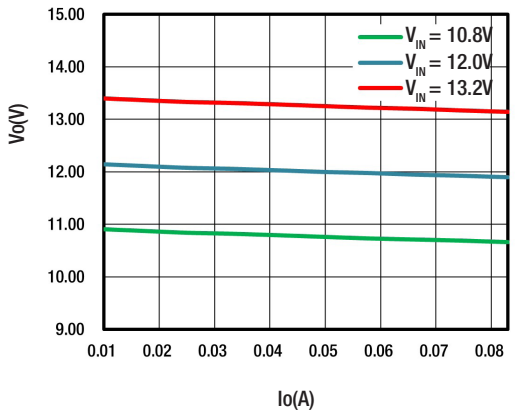


Fig. 5 Output Voltage vs Output Current
(12V to 12V/1W)

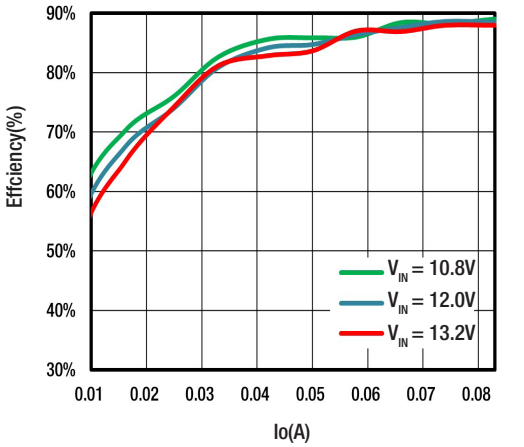


Fig. 6 Conversion Efficiency vs Output Current
(12V to 12V/1W)

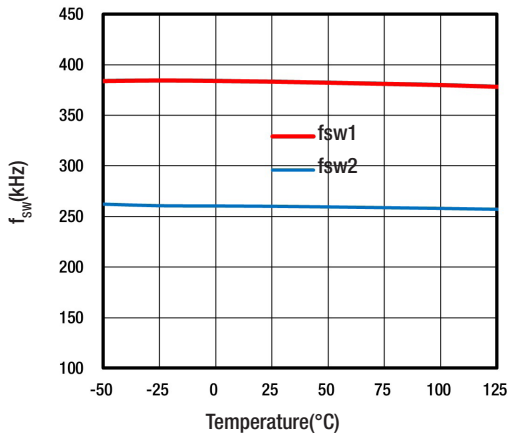


Fig. 7 Frequency vs Temperature

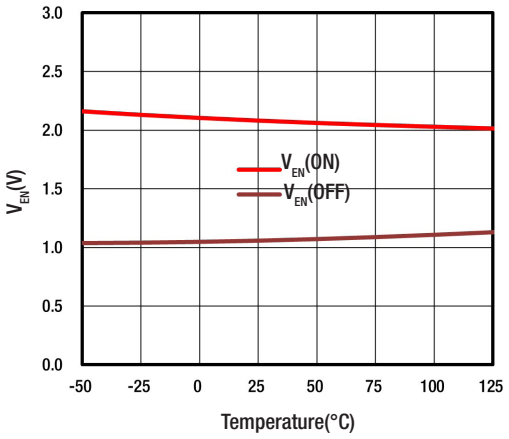


Fig. 8 V_{EN} vs Temperature

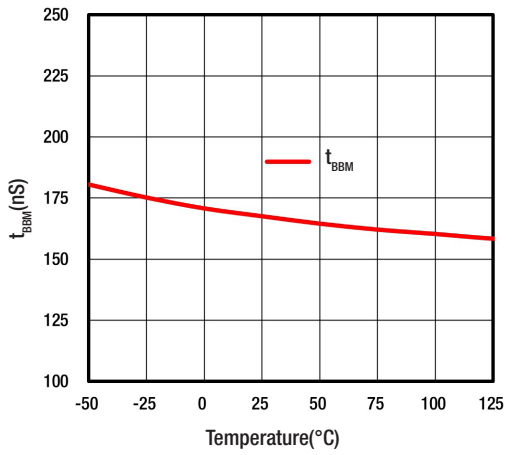


Fig.9 t_{BBM} vs Temperature

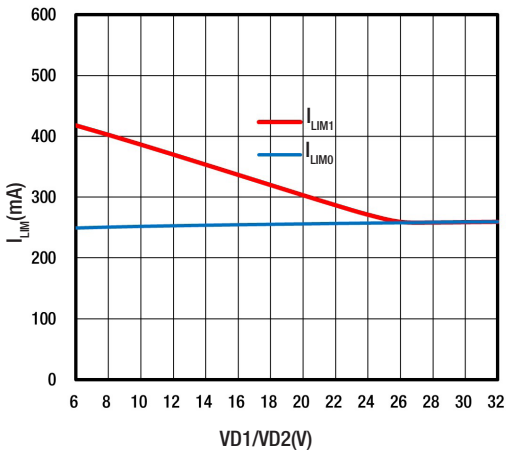


Fig.10 I_{LIM} vs Drain Conduction Voltage

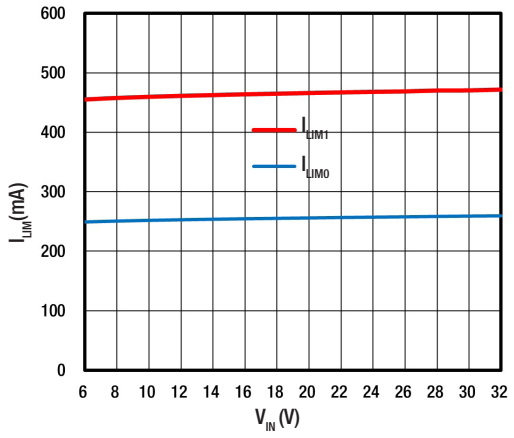


Fig.11 I_{LIM} vs Input Voltage

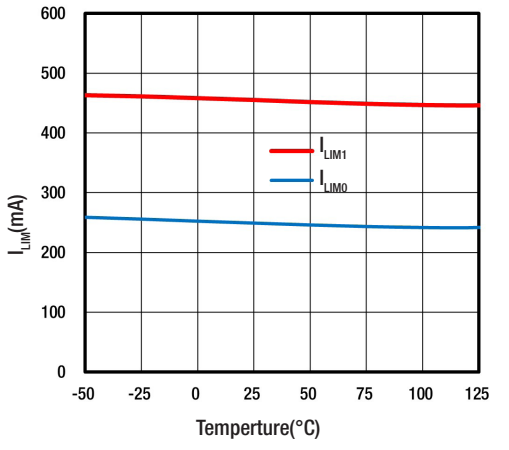


Fig.12 I_{LIM} vs Temperature

PARAMETER MEASUREMENT INFORMATION

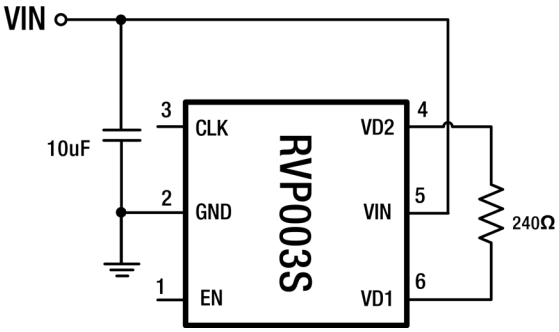


Fig. 13 f_{sw0}/ V_{SLEW}/ t_{BBM} Test Circuit

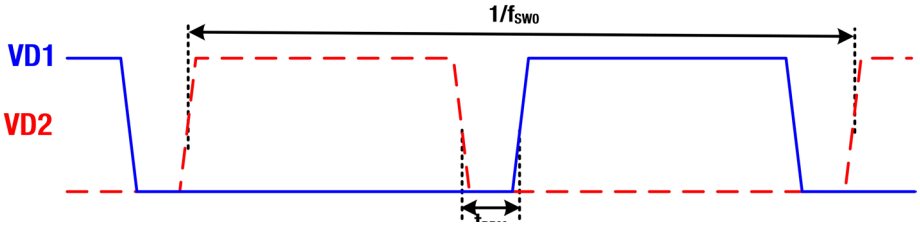


Fig. 14 VD1 and VD2 Timing Diagram

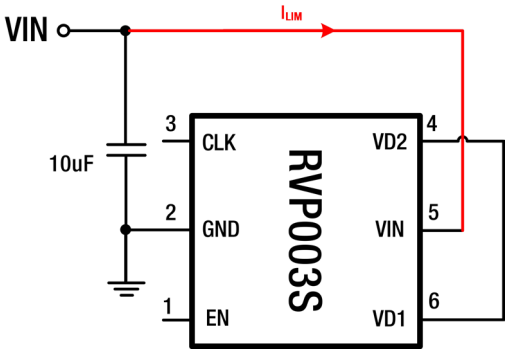


Fig. 15 I_{LIM} Test Circuit

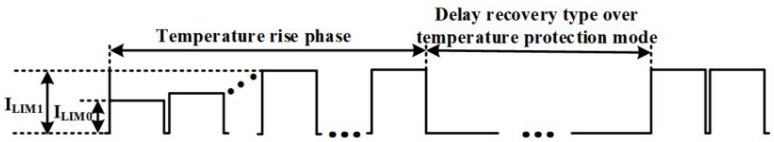


Fig. 16 I_{LIM} Timing Diagram

DETAILED DESCRIPTION

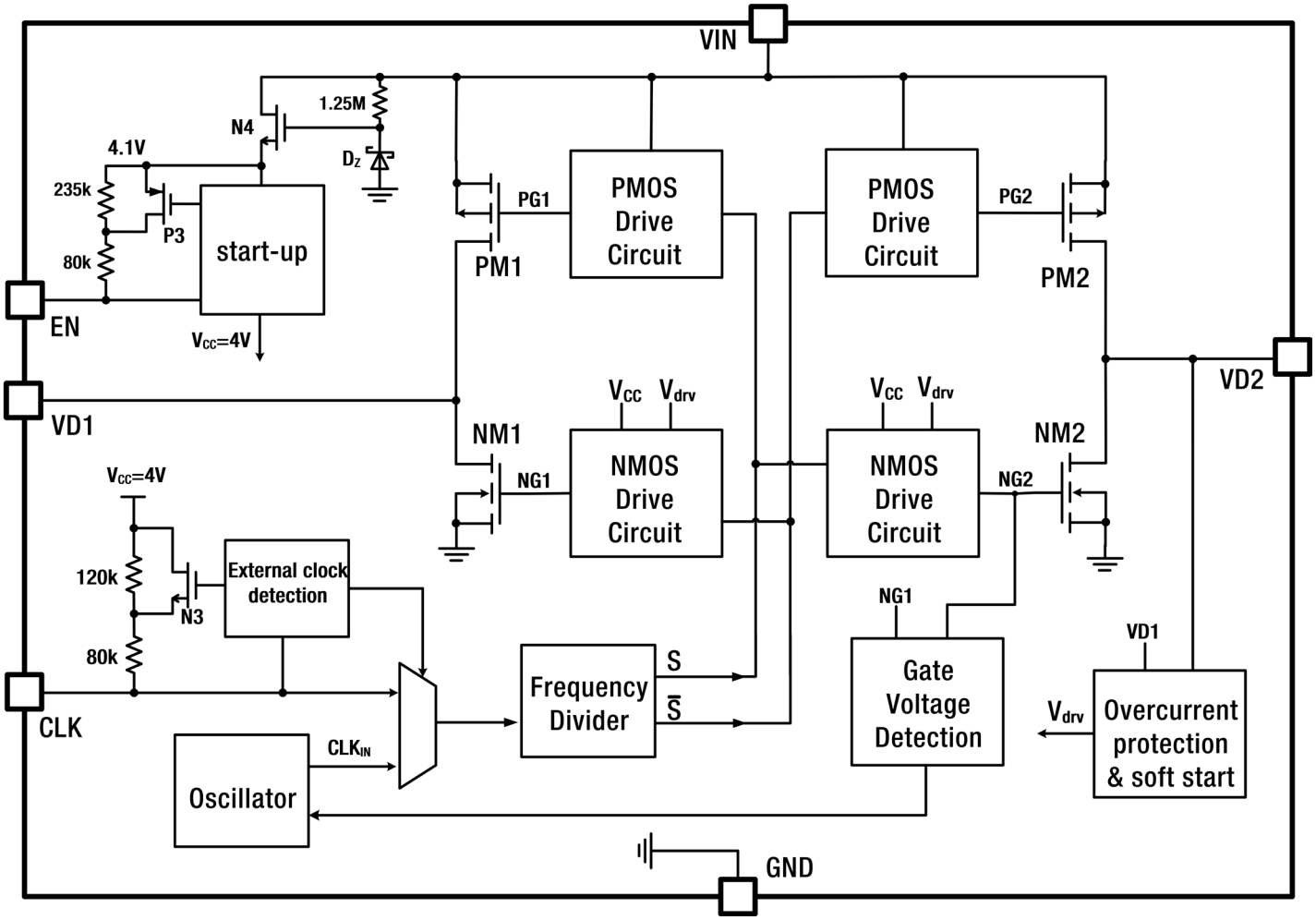
Overview

The RVP003S is an integrated isolated DC-DC switching power supply controller designed for full-bridge topologies. Its bridge-drive architecture minimizes transformer winding requirements, helping reduce system cost while maintaining strong compatibility across a 6V to 30V input voltage range. The device includes a current clamp mechanism that limits the peak current through the power MOSFETs. This not only ensures the internal components operate within safe limits but also protects external circuitry from high-current stress.

The switching frequency is selectable via the CLK pin. When the pin is left floating, the device operates at a lower frequency f_{SW0}; when connected to GND, it switches at a higher frequency f_{SW1}. Alternatively, an external clock can be applied to the CLK pin. In this mode, the controller generates two complementary drive signals at half the frequency of the input clock. An internally defined dead time t_{BBM} is inserted between the drive signals to prevent shoot-through and reduce drain-source voltage stress during switching, minimizing overall switching losses.

Device operation is controlled via the EN pin. When pulled high or left unconnected, as it defaults high-the chip functions normally. Pulling EN low disables the device, placing it in an ultra-low standby power state.

FUNCTIONAL DIAGRAM



OPERATION MODE

Full Bridge Waveform

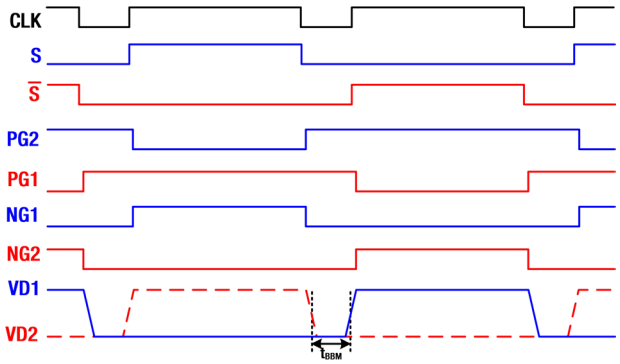


Fig. 17 Output Signal Waveforms

In Figure 17, NG1 and NG2 represent the logic-level gate voltages of power switches NM1 and NM2, respectively. Both signals have equal high-level pulse widths. A brief period occurs between their high states during which both signals remain low-this interval is known as the dead time t_{BBM}. The purpose of t_{BBM} is to prevent shoot-through by ensuring NM1 and NM2 are not on simultaneously, while also allowing the switches to turn on at a lower drain-source voltage to reduce switching losses.

The dead time t_{BBM} is primarily determined by the low-level duration of the internal oscillator clock (CLK) and varies with the operating frequency: lower switching frequencies result in longer dead times, while higher frequencies shorten it. Additionally, t_{BBM} is generated only after confirming that both NM1 and NM2 have fully turned off by monitoring their gate voltages. This approach minimizes the impact of gate-drive delays and temperature variations, ensuring consistent dead time performance across the full input voltage range.

Current Clamp Mode

During converter start-up, if the output is short-circuited or the transformer becomes magnetically saturated, the current through the power switches may rise excessively. To prevent damage, the device monitors this current and, if it exceeds the defined current clamp limit I_{LIM}, it reduces the gate drive voltage of switches NM1 and NM2, effectively limiting the current. This current-limiting mechanism ensures safe operation of the power switches and protects both the transformer and output rectifier diode from high current stress, thereby enhancing the overall reliability of the converter.

Delay Recovery Overtemperature Protection Mode

When the internal temperature of the chip exceeds the predefined threshold, the device enters an overtemperature protection mode. In this state, all power switches are disabled to prevent further heating. To resume normal operation, two conditions must be met: 1. The internal temperature must drop below the recovery threshold. 2. A mandatory cool-down period must elapse. This protection mechanism ensures that, upon restart, the internal chip temperature is closer to ambient temperature. As a result, when the device approaches the overtemperature threshold again, it benefits from a wider thermal margin. This allows the power switches to remain active for a longer duration, improving their ability to handle larger capacitive loads and preventing abnormal behavior during restart particularly in systems with high output capacitance.

Principle of Output Short Circuit Protection

The full bridge converter implements output short-circuit protection through the combined mechanisms of current clamp control and delayed-recovery overtemperature protection. When an output short circuit occurs, the transformer's primary winding (N_P) experiences a limited voltage drop, while most of the input voltage (VIN) is dropped across the N-channel MOSFETs. Upon detection of excessive current, the chip activates the current clamp mode, limiting the gate drive and thus the current through the power switches. As a result of continuous clamping, the chip's internal temperature gradually increases, eventually triggering the overtemperature protection mode. This mode includes a delayed recovery mechanism, allowing the device to cool before reactivating. The rate at which the chip heats up-and thus how quickly overtemperature protection is triggered-depends on ambient conditions and input voltage. Lower ambient temperatures or reduced input voltages slow the temperature rise, extending the time before shutdown and effectively increasing the converter's ability to handle capacitive loads. Even in high temperature environments, the delayed recovery feature improves stability and startup behavior under heavy capacitive loading.

General Operating Mode

During start-up, the output capacitor initially holds a low voltage, causing a relatively high inrush current through the power switches. To protect the circuit, the converter starts in current clamp mode, limiting the current to a safe level. As the output voltage approaches its rated value, the current drawn by the power switches decreases. At this point, the drive voltage to the switches increases, reducing their ON-resistance $R_{DS(ON)}$ and improving overall efficiency

EN Shutdown Mode

The Zener diode (DZ), NMOS transistor N4, and a 1.25MΩ bias resistor form a 4.1V voltage source that provides the bias voltage for the EN (enable) pin. Internally, the EN pin is connected to a pull up resistor network consisting of 235kΩ and 80kΩ resistors in series. When the EN voltage exceeds the enable threshold voltage $V_{EN(ON)}$, the device (e.g., RVP003S) enters normal operation, and PMOS transistor P3 turns on. In this state, the effective pull-up resistance at the EN pin becomes 80kΩ, enhancing noise immunity. If the EN voltage falls below the disable threshold voltage $V_{EN(OFF)}$, the chip shuts down its output, an PMOS P3 turns off. This increases the equivalent pull up resistance at the EN pin to 315kΩ, thereby reducing standby power consumption. The temperature characteristics of $V_{EN(ON)}$ and $V_{EN(OFF)}$ are illustrated in the function block diagram.

Operating Frequency Selection

The CLK pin supports clock synchronization. When an external clock signal is applied to CLK, the device uses an internal frequency divider to generate complementary drive signals, allowing the RVP003S to operate at half the frequency of the input clock.

The RVP003S also includes an internal oscillator. If the input to the CLK pin remains continuously high or low for six internal clock cycles, the device automatically switches to its internal clock as the operating frequency. When the CLK pin is left floating, the internal oscillator defaults to low-frequency mode f_{SW0}. If CLK remains in a high state for six full f_{SW0} cycles, f_{SW0} is confirmed as the active switching frequency. When the CLK pin is connected to GND, the internal oscillator runs at a higher frequency f_{SW1}. If CLK remains low for six full f_{SW1} cycles, the device automatically selects f_{SW1} as the operating frequency. This mechanism ensures smooth automatic selection between internal and external clocks, depending on CLK pin behavior.

Full Bridge Converter

Operating Principle Of Full Bridge Converter

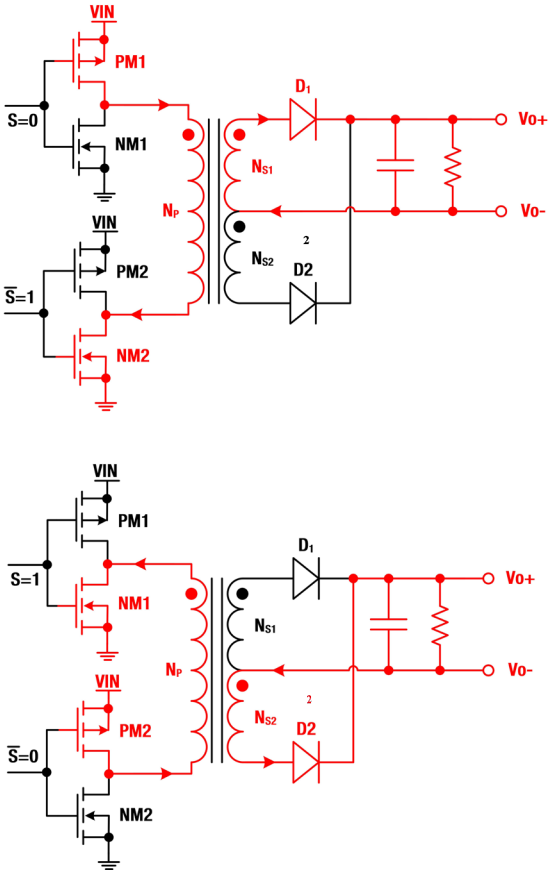


Fig. 18 Full Bridge Transformer Schematic

When S=0, P-channel MOSFET PM1 and N-channel MOSFET NM2 are turned on, while PM2 and NM1 are turned off, establishing the first direction of isolated power transfer. On the primary side of the transformer, current flows from the positive terminal (VIN) of the input power supply through PM1, into the dotted end of the primary winding N_P, exits from the non-dotted end, and then flows through NM2 to ground (GND).
On the secondary side, current flows into the non-dotted end of winding N_{S1}, exits from the dotted end, and passes through rectifier diode D_1 to the output terminal. During this phase, no current flows through N_{S2}, and diode D_2 remains off.
When S=1, PM2 and NM1 are switched on, while PM1 and NM2 are turned off, establishing the second direction of isolated transmission. In this state, current flows from VIN through PM2, into the non-dotted end of the primary winding N_P, exits from the dotted end, and then flows through NM1 to GND. On the secondary side, current flows into the dotted end of winding N_{S2}, exit from the non-dotted end, and is delivered to the output terminal through diode D_2, while N_{S1} is inactive and diode D_1 is off. The full-bridge converter operates with an almost 100% duty cycle, enabling efficient energy transfer and excellent dynamic performance. After rectification, only a small output filter capacitor is theoretically needed to maintain low output voltage ripple. However, to prevent shoot-through between switches during transitions on the primary side and to minimize switching losses, the controller introduces a dead time between switching phases. During this interval, no power is transferred from the transformer, and the output capacitor temporarily supplies energy to the load, resulting in a slightly increased output voltage ripple.

Core Magnetization

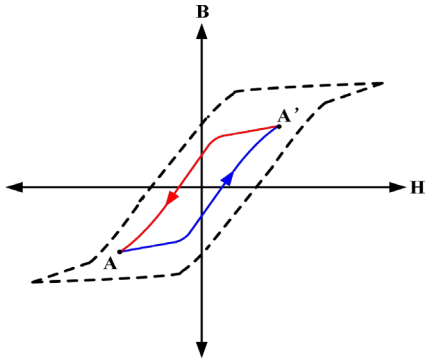


Fig. 19 Full Bridge Transformer Core Magnetization

For a full bridge transformer to function properly, it must satisfy the volt-second balance condition. This means the volt-second product (the product of voltage and time) during the excitation phase must equal that of the demagnetization phase. If this balance is not maintained, core saturation may occur. The transformer's magnetic behavior is illustrated by the B-H curve in Figure 19, where B represents the magnetic flux density, and H denotes the magnetic field strength within the core. When PM1 and NM2 are turned on, the transformer enters the excitation phase. During this time, magnetic flux density increases as the core is driven from point A to A' on the B-H curve. When these switches are turned off, the flux reaches its maximum positive value at A'. Next, when PM2 and NM1 are turned on, the transformer enters the demagnetization phase, and the magnetic flux density decreases as it moves back from A' to A. When these switches are turned off, the flux reaches its maximum negative value at A. The change in magnetic flux density B is primarily governed by the volt-second product V_P x T_{ON}, where Vp is the voltage across the primary winding and T_{ON} is the duration for which the voltage is applied. To maintain normal operation, the volt-second product during excitation must equal that during demagnetization. If this condition is not met, it results in magnetic bias-a gradual shift of the core's operating point in one direction. Over time, this bias causes the core's flux density to drift toward saturation. Once the core exceeds its saturation limit, it can no longer support proper magnetic energy transfer, leading to transformer malfunction or failure.

TYPICAL APPLICATION

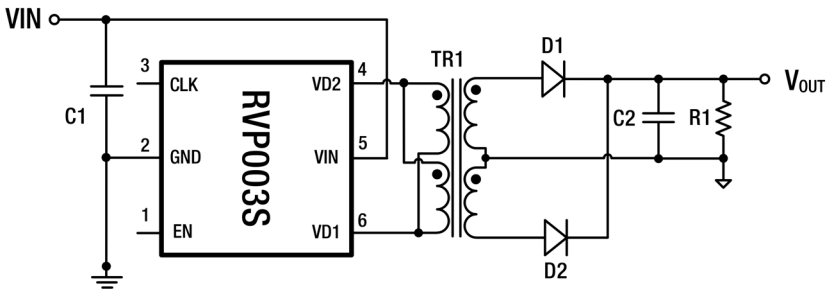


Fig. 20 Typical Application Schematic

Design Requirements

The following are typical application circuits designed for an input voltage of 12V ±10%, providing an isolated, unregulated 5V output with a maximum output power of 1W. The technical specifications of the power supply are detailed below:

Input and Output Parameters

Specification	MIN	TYP	MAX	UNIT
Input Voltage	10.8	12.0	13.2	V
Output Voltage	---	5.0	---	V
Output Current	---	0.2	---	A
Output Ripple and Noise	---	50	100	mV
Voltage Regulation	---	---	1.5	%
Load Regulation	---	---	10	%
Conversion Efficiency	---	85	---	%
Reliability Requirements				
Output Short Circuit Protection	Continuous, self-recovery			
Operating Temperature	-40	---	85	°C
Isolation	3000	---	---	VDC

Input Capacitor Selection

As shown in Figure 20, the input capacitor C1 serves multiple purposes, including energy storage, filtering, and decoupling. For enhanced decoupling performance, an additional 0.1µF ceramic capacitor can be connected in parallel between VIN and GND, positioned as close to the chip as possible. During converter operation, C1 supplies transient current to the circuit. To minimize input voltage ripple, a capacitance value between 1µF and 10µF is recommended. The capacitor's voltage rating must exceed the maximum expected input voltage to ensure reliable operation. For improved reliability and performance, ceramic chip capacitors with low ESR and stable temperature characteristics are recommended to account for derating effects. For optimal filtering performance, C1 should be placed as close to the device as possible, and power loop traces should be short and wide. This minimizes voltage spikes caused by high-frequency switching currents and the inductance of PCB traces during operation.

Output Rectifier Diode Selection

For the output rectification circuit, it is recommended to use Schottky diodes with low forward voltage drop and short reverse recovery time, which help achieve better load regulation and higher conversion efficiency. This design uses a full-wave rectifier topology, where the rectifier diode experiences a reverse voltage stress approximately twice the output voltage. Therefore, the diode's reverse voltage rating should be at least twice the maximum output voltage, with appropriate derating The output rectifier diode must also meet the device's operating temperature range requirements. Notably, at high temperatures, the reverse leakage current of Schottky diodes increases significantly, so careful derating based on the diode's temperature characteristics (as shown in its temperature derating curve) is necessary. To ensure reliable and stable operation of the full bridge converter under all conditions, the diode selection must also consider the maximum operating current during abnormal short-circuit events at the output. When the RVP003S enters output short-circuit protection mode, it automatically switches to current clamp mode to limit the MOSFET's current to the clamp limit I_{LIM} (typically 450mA, maximum 600mA). The maximum operating current rating for the output rectifier diode can be calculated using the transformer turns ratio with the following equation:

$$I_{D-MAX} = \frac{N_P}{N_S} \times I_{\mathrm{LIM-MAX}}$$

In the equation, N_P and N_S represent the number of turns on the primary and secondary windings of the full bridge transformer, respectively, and $I_{LIM-MAX}$ is the maximum current clamp limit of the chip. During protection mode, the converter enters overtemperature protection with delayed recovery. In this phase, once the chip transitions to self-recovery and then re-triggers overtemperature protection, the output rectifier diode experiences its maximum operating current. Therefore, when selecting the rectifier diode, it is essential to ensure its peak forward surge current I_{FSM} can handle these stress conditions. For this application, the RB160M-30 Schottky diode is a suitable choice. At an operating temperature of 75°C, it features:

- A forward voltage drop of approximately 280mV @ 0.2A
- A reverse leakage current of about 90µA @ 15V
- A peak forward surge current rating I_{FSM} of 30A

If the design requires operation at higher ambient temperatures, it is advisable to choose a Schottky diode with lower reverse leakage current under elevated temperatures to maintain performance and reliability.

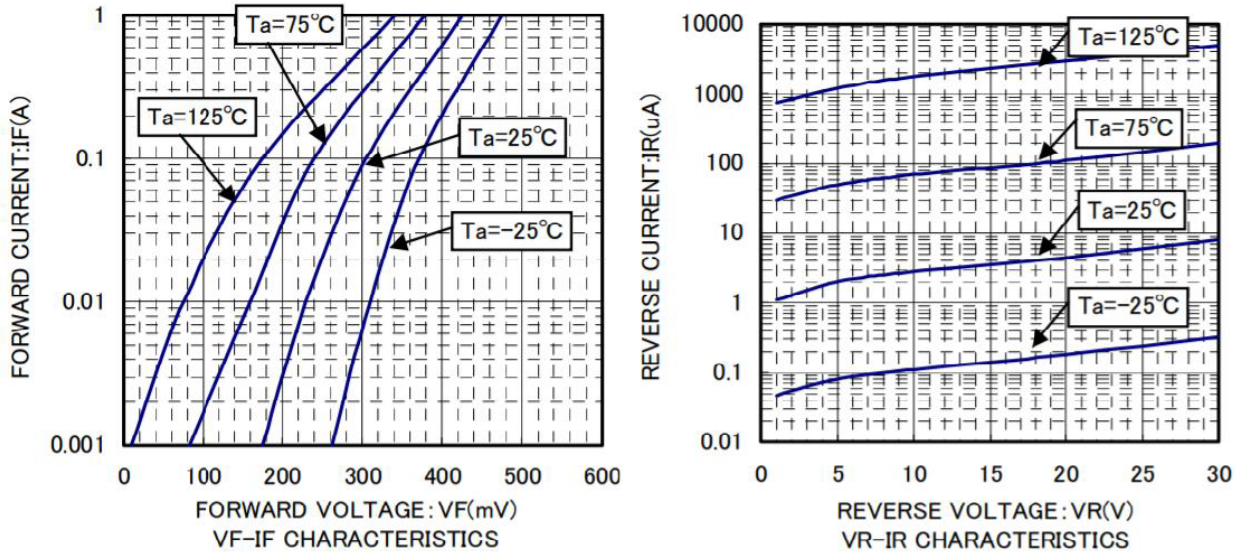


Fig. 21 Schottky Diode RB160M-30 Characteristics

Output Capacitor Selection

In theory, a full bridge converter can achieve 100% duty cycle, continuously transferring power to the secondary side. However, to ensure safe and reliable operation, a short dead time is introduced during switching transitions between bridge legs to prevent shoot-through (shorting). During this dead time, energy is not transferred from the transformer; instead, the output filter capacitor (C2) supplies power to the load, which leads to a certain amount of output voltage ripple. To minimize this ripple and improve filtering performance, it is recommended to use a 4.7µF to 10µF ceramic capacitor for C2.

Full Bridge Transformer Selection

Estimating the Primary-to-Secondary Turns Ratio Once the output rectifier diode has been selected based on the design, its forward voltage drop VF at maximum output load can be determined. The primary-to-secondary winding turns ratio of the full bridge transformer can then be estimated using the input voltage across the primary winding and the minimum required voltage on the secondary side.
Under nominal input voltage and full-load conditions, the voltage across the primary winding is:

$$V_p = V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} (R_{DSP(ON)} + R_{DSN(ON)})$$

P_{O-MAX} is the maximum output power of the full-bridge converter, η is the estimated nominal conversion efficiency at full load, and $R_{DSP(ON)}$ and $R_{DSN(ON)}$ are the ON-resistances of the PMOS and NMOS switches, respectively.
At full output load, the minimum output voltage of the secondary winding is:

$$V_S = V_{O-MIN} + V_F$$

V_{O-MIN} is the minimum output voltage permitted by the full bridge converter at full load. To ensure the output voltage curve meets the specification, V_{O-MIN} is calculated as 97% of the nominal output voltage (nominal output voltage minus 3% tolerance). VF represents the forward voltage drop of the selected output rectifier diode at full load.
Based on the above equation, the primary-to-secondary turns ratio can be determined as follows:

$$N_{PS} = \frac{V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} \times (R_{DSP(ON)+}R_{DSN(ON)})}{V_{O-MIN+}V_F}$$

Based on the input and output requirements of this application, the primary and secondary turns ratio is approximated as:

$$N_{PS} = \frac{12 - \frac{1}{0.85 \times 12V} \times (0.60\Omega + 0.25\Omega)}{5V \times 0.97 + 0.34V} = 0.34$$

Volt-second Product Calculation

To prevent transformer saturation, the volt-second product of the transformer must exceed the maximum volt-second product generated by the RVP003S under all normal operating conditions. For applications with a narrow input voltage range, typically ±10% of the nominal input voltage, the volt-second product should be calculated based on the upper limit of the input voltage. Additionally, the chip's frequency and tolerance must be taken into account to ensure saturation does not occur at the minimum operating frequency. The maximum volt-second product applied to the transformer's primary winding occurs when the minimum operating frequency corresponds to half of the switching cycle at the highest input voltage.
Consequently, the minimum volt-second product can be calculated as follows:

$$Vt_{MIN} \geq V_{IN-MAX} \times \frac{T_{MAX}}{2} = \frac{V_{IN-MAX}}{2 \times f_{MIN}}$$

Based on the design requirements of this application, the operating frequency of RVP003S is typically 250KHz and the minimum operating frequency is 225KHz. When the input voltage is at the highest, the volt-second product should be:

$$Vt_{MIN} \geq \frac{13.2V \times 110\%}{2 \times 225kHz} = 16\mu s$$

The selection of the full bridge transformer should be based on the specific application requirements, including the appropriate volt-second product and turns ratio. Additionally, factors such as maximum output power, isolation voltage ratings, and distributed isolation capacitance must also be carefully considered.

RVP003S Transformer Driver for Micro-power Isolated Supplies

6-30VIN/30V/0.3A Power Switch

TYPICAL APPLICATION CIRCUIT

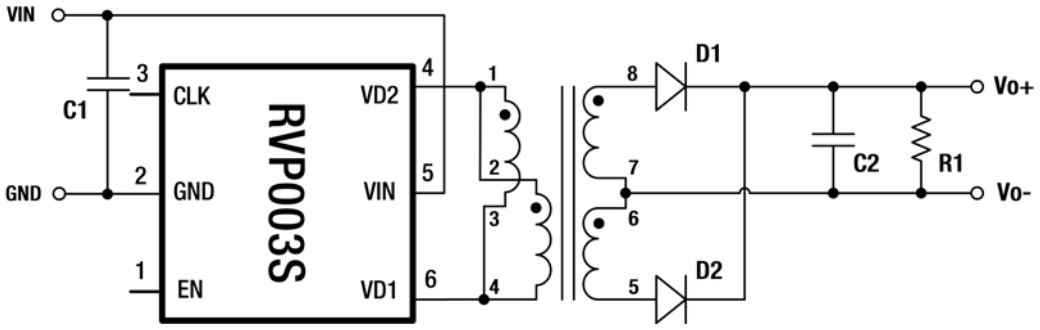
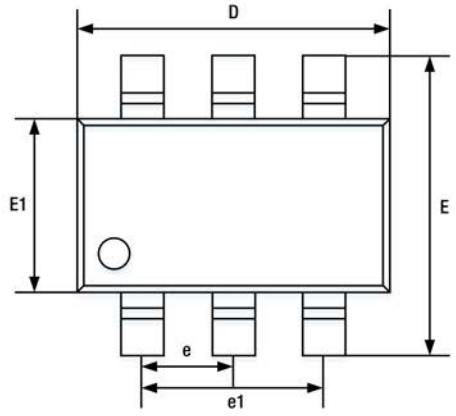


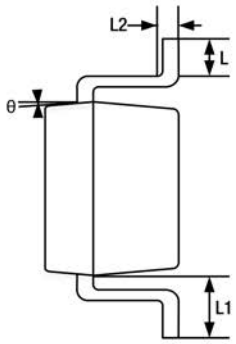
Fig. 22

V_{IN} (V)	V_{OUT} (V)	Power (W)	Isolation Voltage	Reference
12	5	1	3000 VDC	Fig.22

PACKAGING INFORMATION

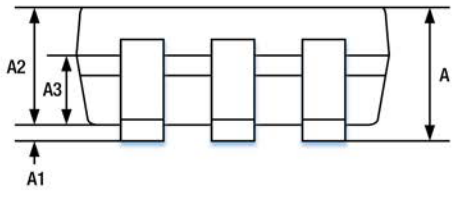


top view

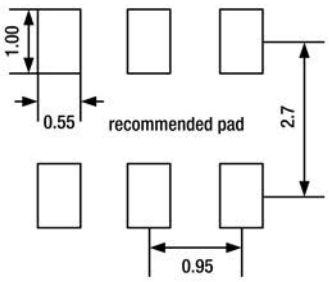


side view

DIMENSION TABLE			
SYMBOL	MILLIMETER		
	MINIMUM	NOMINAL	MAXIMUM
A	---	---	1.25
A1	0.00	---	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
θ	3°	5°	7°



front view



ORDER INFORMATION

Device	Package Type	PIN	Packaging Method	QTY	Marking Code*	MSL
RVP003S-FBN-R	SOT23-6	6	Tape and Reel	3000	RVP003S	MSL-3

*Marking Code :
RVP003S—— Product Code